

GIGABYTE GA-8IPE1000 Pro-G Schematics

Revision 3.1

SHEET

TITLE

SHEET

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03	BLOCK DIAGRAM
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06	P4_478C
07	SPRINGDALE HOST
08	SPRINGDALE DDR
09	SPRINGDALE AGP, HUB, CSA, VGA
10	SPRINGDALE PWR
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13	DDR TERMINATION
14	AGP 8X SLOT
15	ICH5 PCI, USB, HUB, LAN
16	ICH5 IDE, GPIO, SATA, CTRL
17	ICH5 VCC, GND
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19	ICS952635 CLOCK GENERATOR
20	PCI SLOT1/SLOT2
21	PCI SLOT3/SLOT4/RESET BUFFER
22	PCI SLOT5/SLOT6

23	AC '97 CODEC
24	AUDIO JACK, L_OUT, F_AUDIO
25	ITE 8712/IR_CIR/SCR/S_IRQ
26	COMA/VGA_COMB/LPT
27	IDE1/IDE2/FDD
28	FAN/HW MONITOR
29	KB_MS/GAME/FUSEVCC
30	FRONT PANEL
31	R_USB/F_USB1/F_USB2
32	DDR/VDDQ/5VDUAL/VCCVID POWER
33	VCORE POWER
34	ATX/ATX_12V/FAN1655M
35	MARVELL 88E8001
36	TI TSB43AB23(1394)
37	PCI ROUNTIONG
38	GPIO PIN LIST

PROCESS: C

COMPONENT SIDE (0.5 oz. Copper)
VCC SIDE (1 oz. Copper)
GND SIDE (1 oz. Copper)
SOLDER SIDE (0.5 oz. Copper)

GIGABYTE CORP.

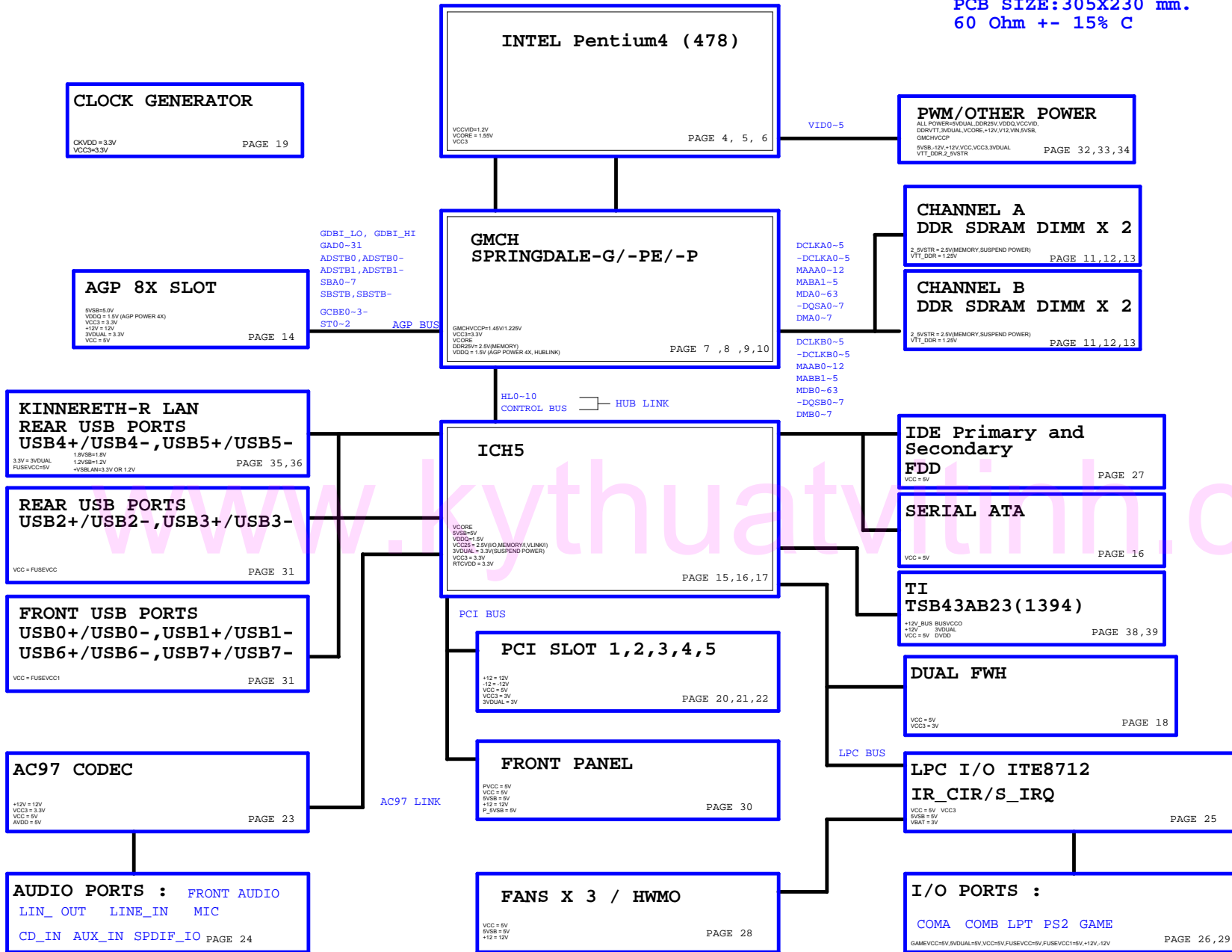
Title: COVER SHEET

Size: Custom Document Number: GA-8IPE1000 Pro-G Rev: 3.1

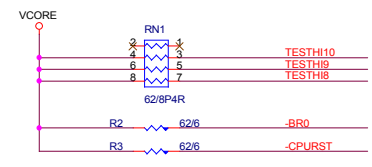
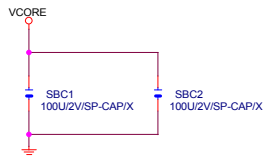
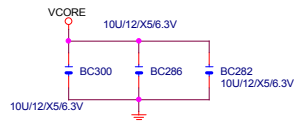
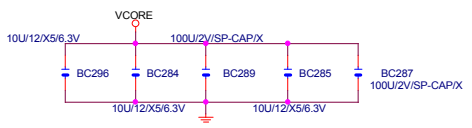
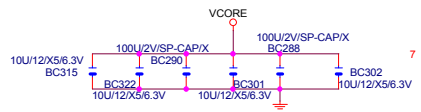
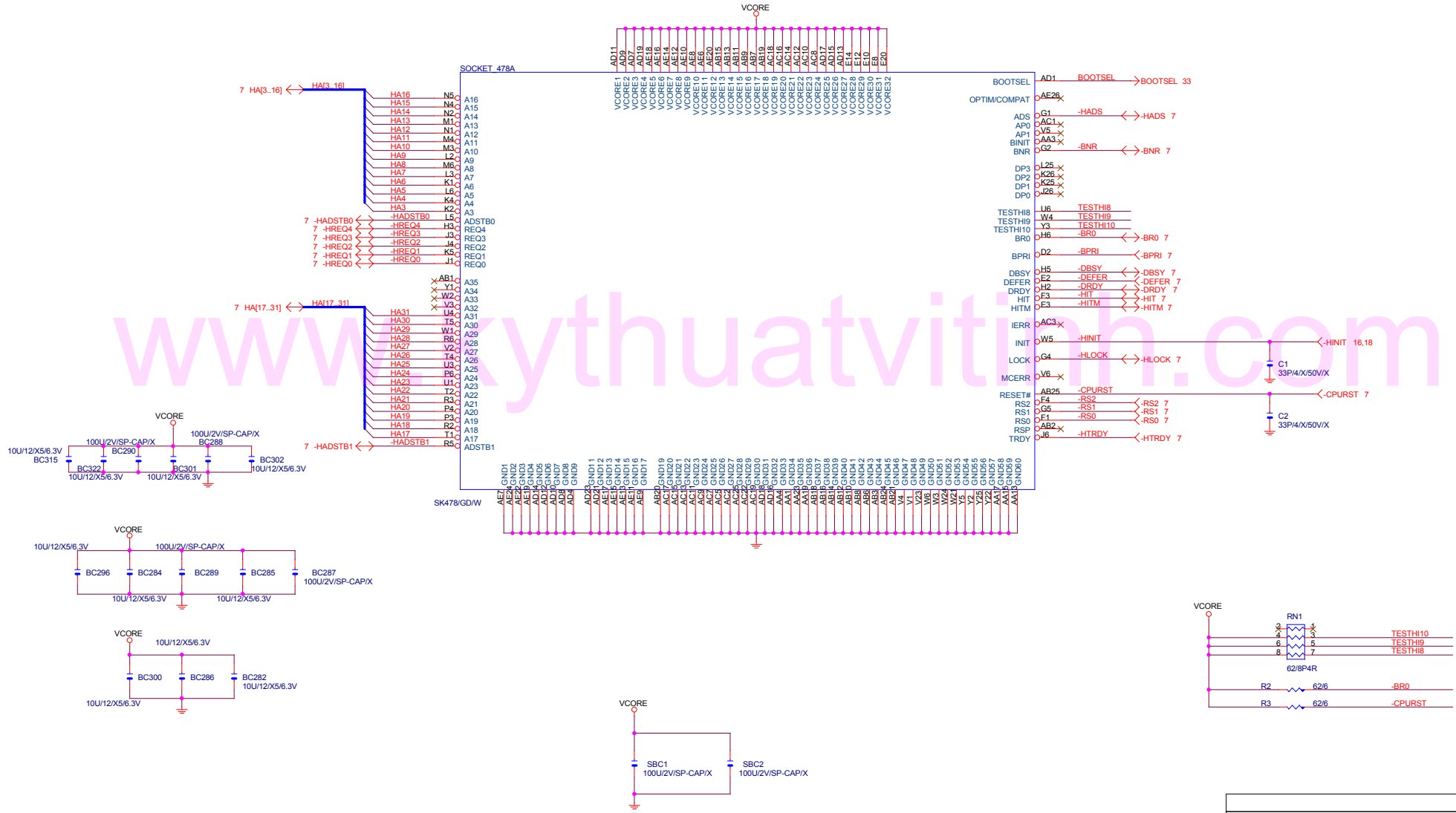
Date: Sheet 1 of 39

BLOCK DIAGRAM

PCB SIZE: 305X230 mm.
60 Ohm +/- 15% C



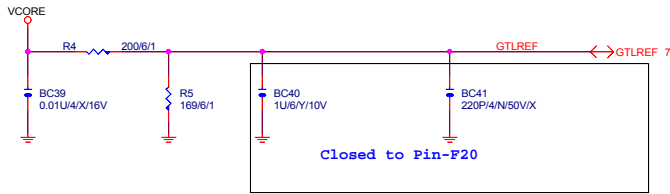
GIGABYTE CORP.			
BOM & PCB MODIFY HISTORY			
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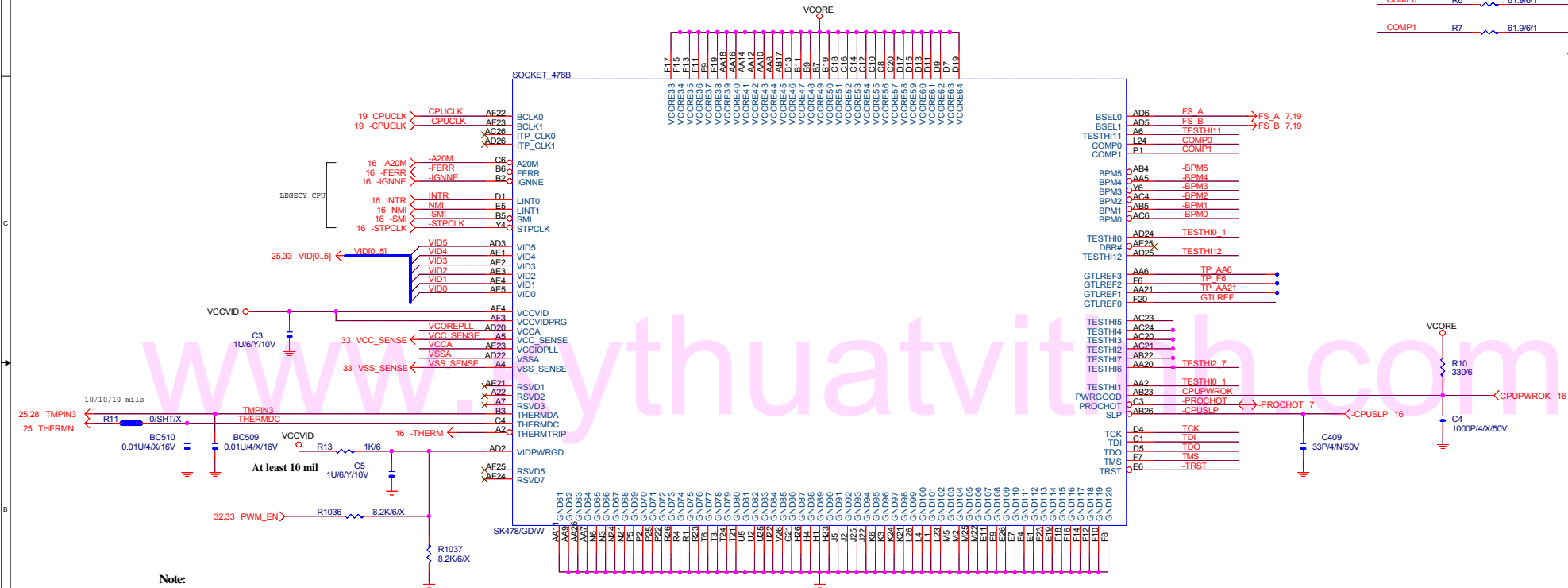
SP-CAP X 4 PCS
CPU SCKET

CAP place at (D14,D15) solder side

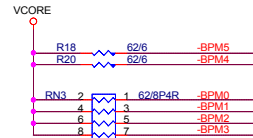
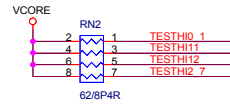
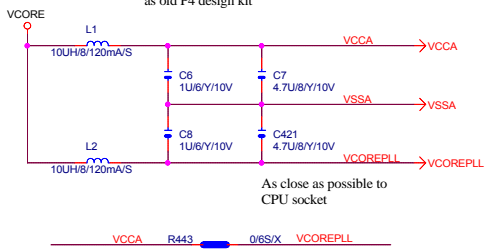
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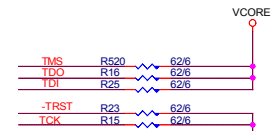
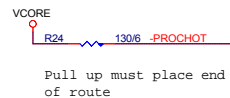
Place outside of CPU socket



Note:
VCCA & VCCOREPLL define doesn't same as old P4 design kit

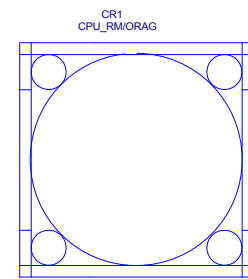
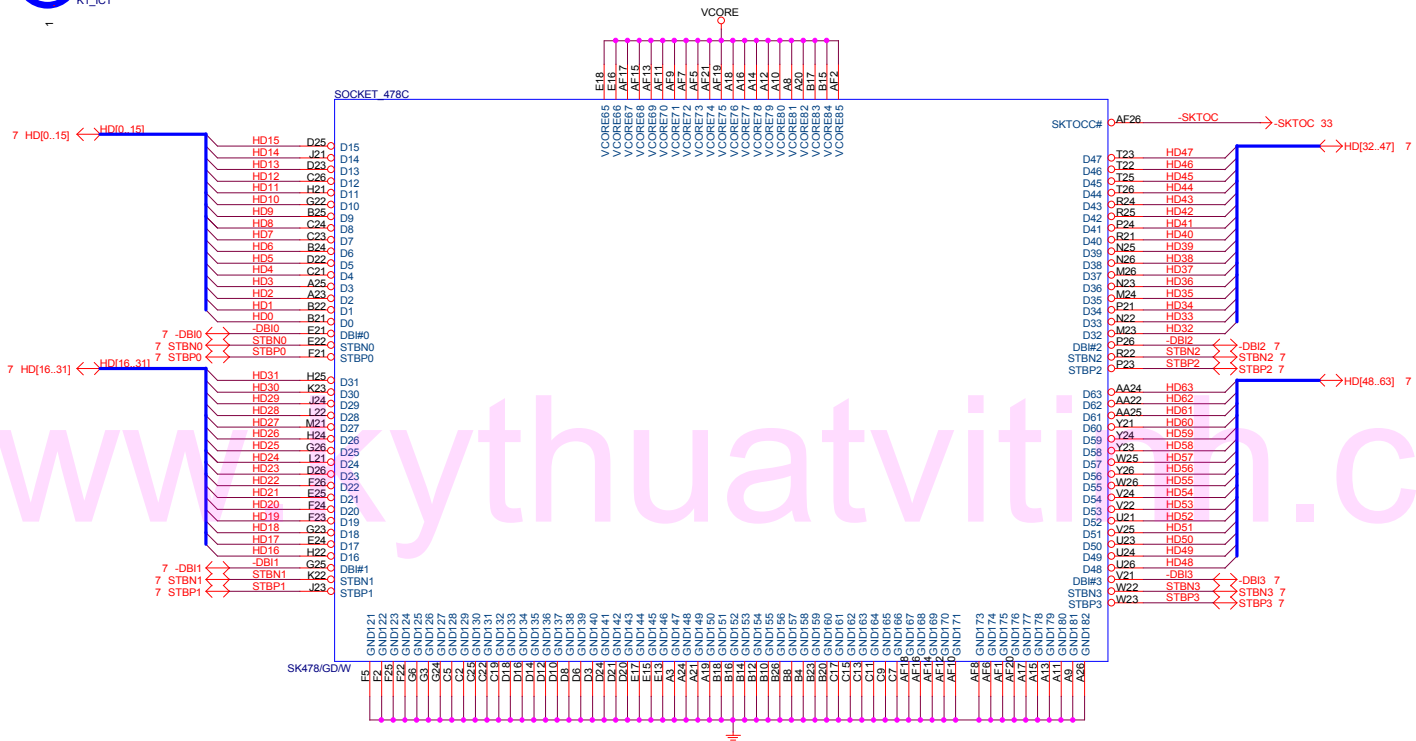
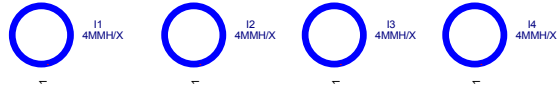
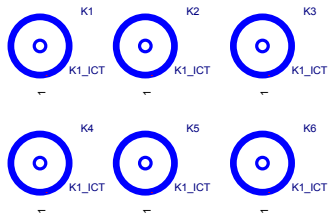


Close to CPU

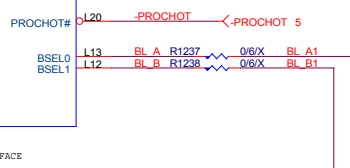
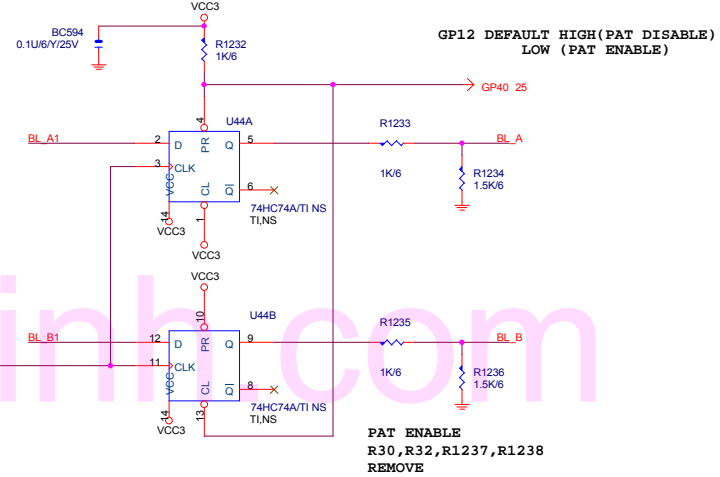
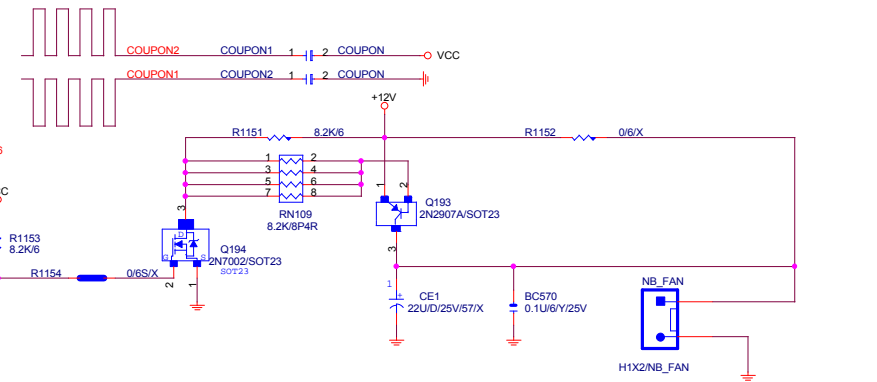
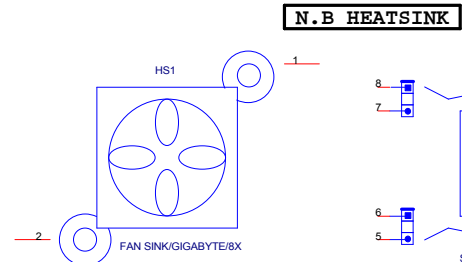
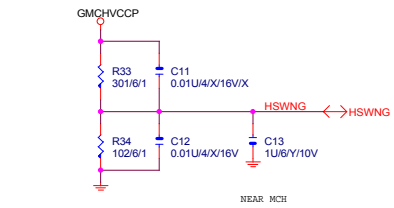
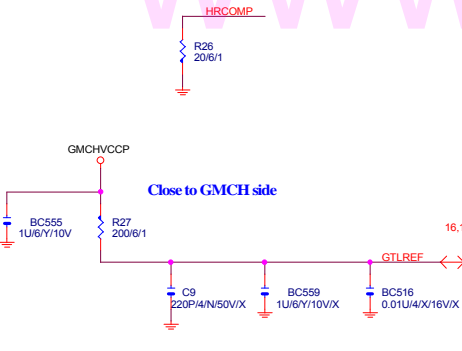
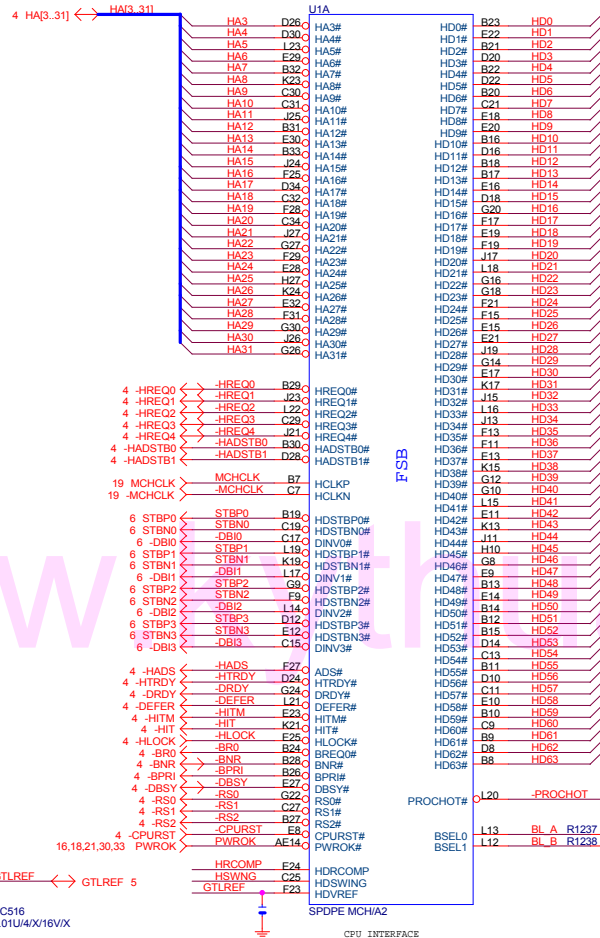


Close to CPU

Title			P4 478B		
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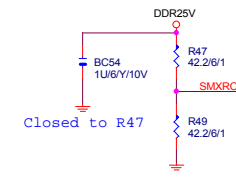
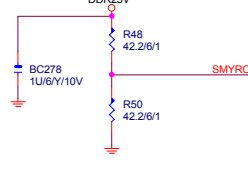
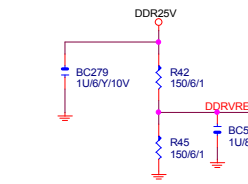
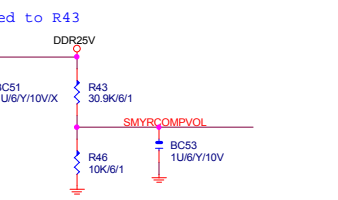
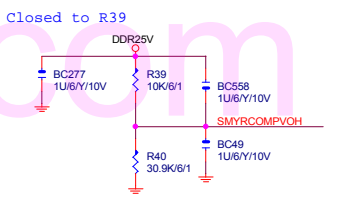
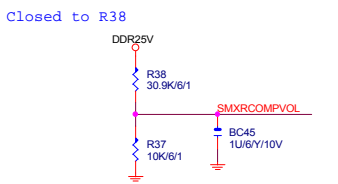
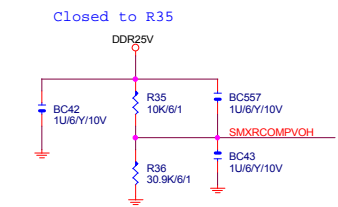
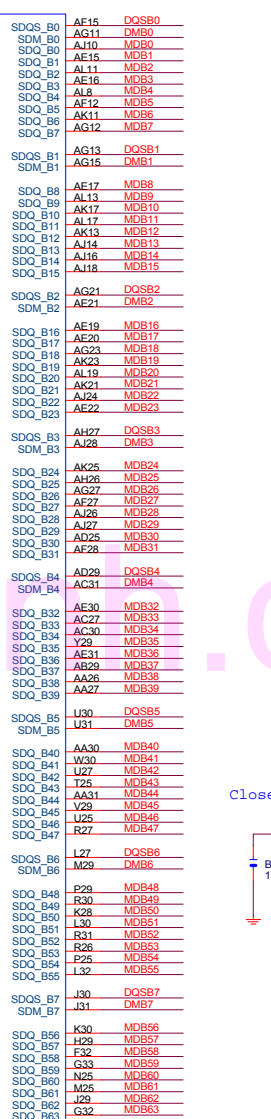
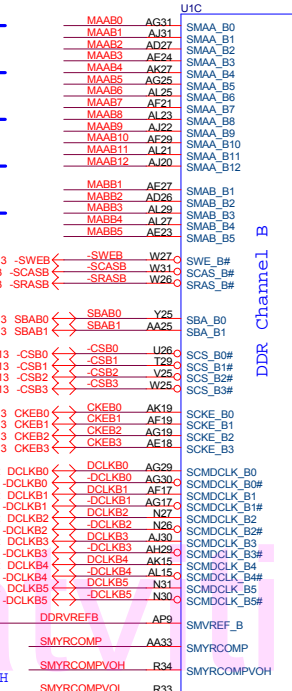
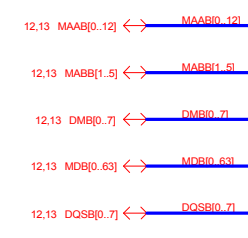
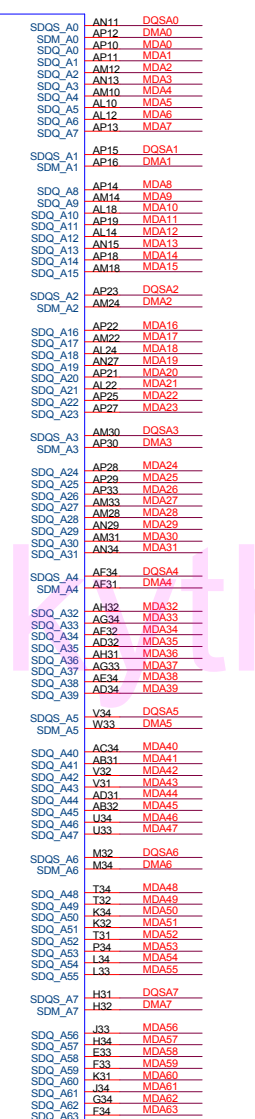
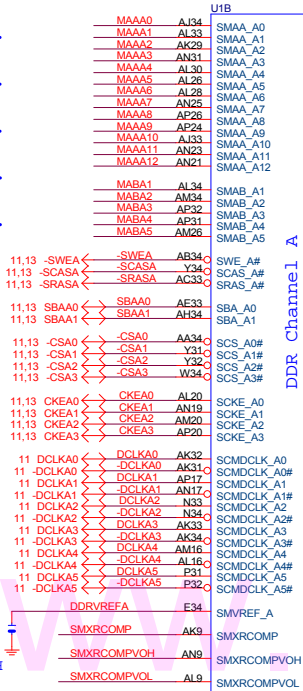
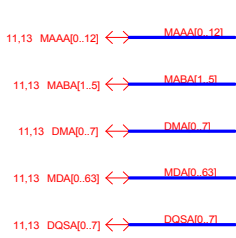
Title			P4 478C		
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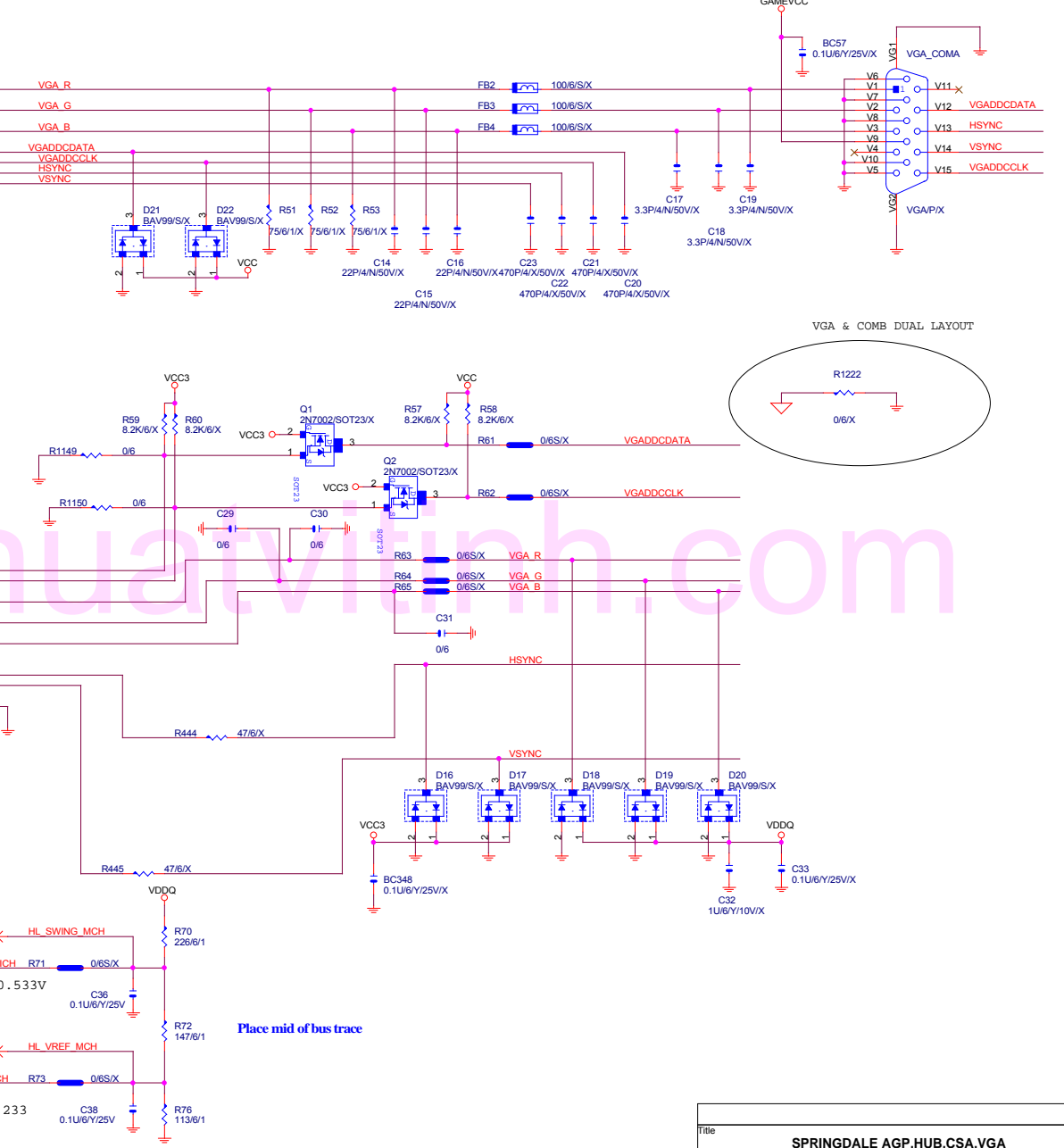
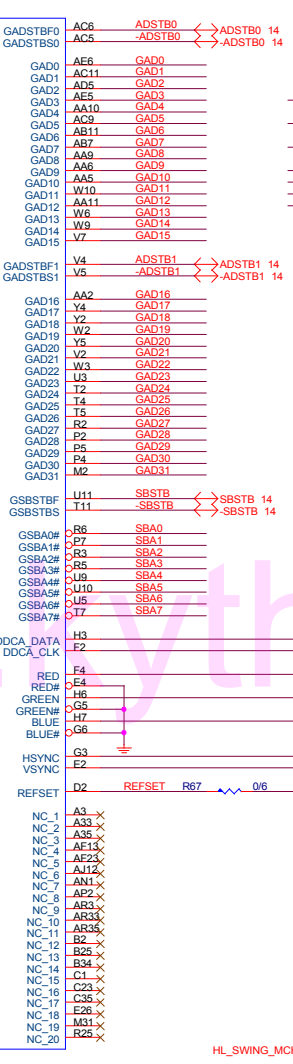
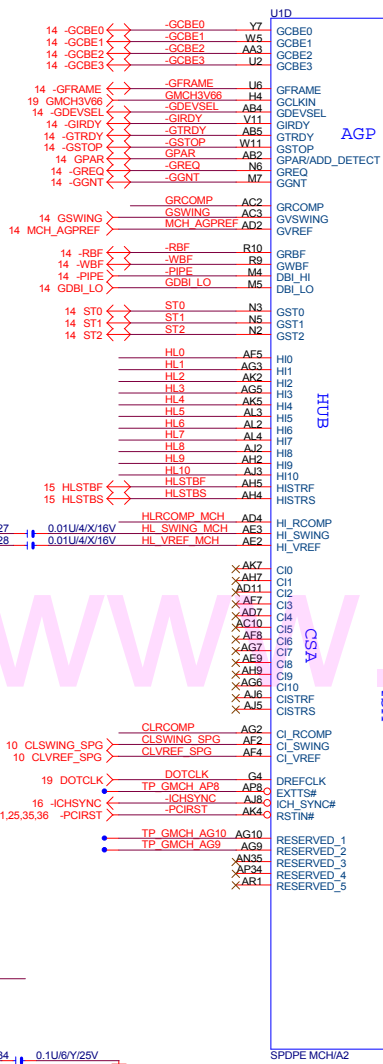
	100	133	200
FS_A	L	H	L
FS_B	L	L	H
X2 (NO)	X2	X2	X1.33
	X2.66	X2.5	X1.6
			X2

FOR SPD P (533MHZ)
REMOVE R28,R31
ADD R1163,U39,

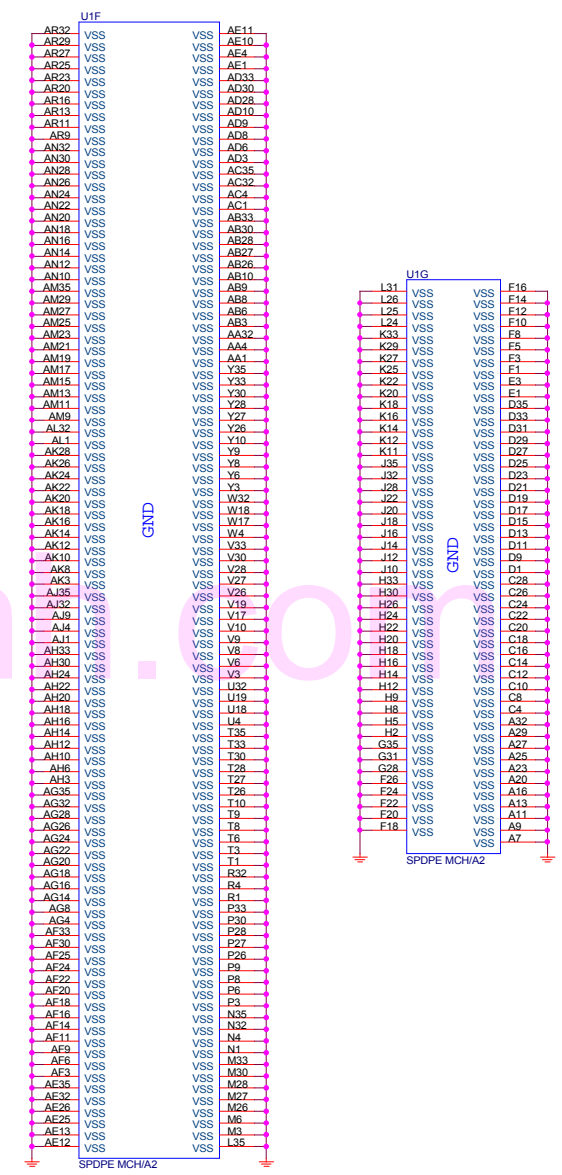
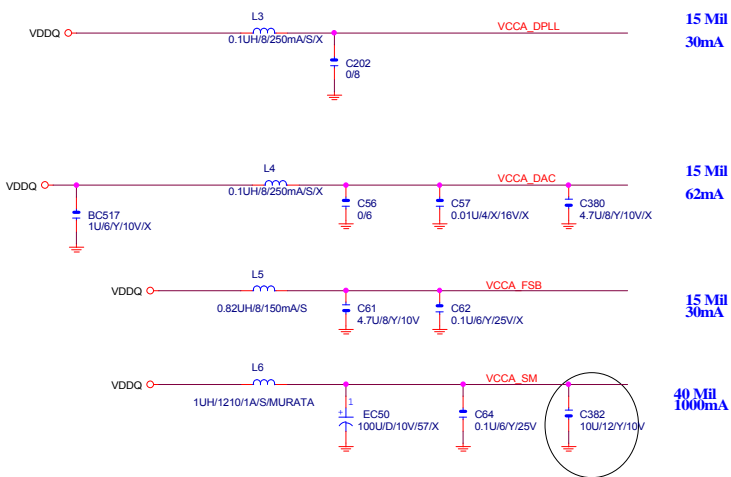
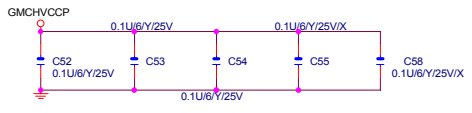
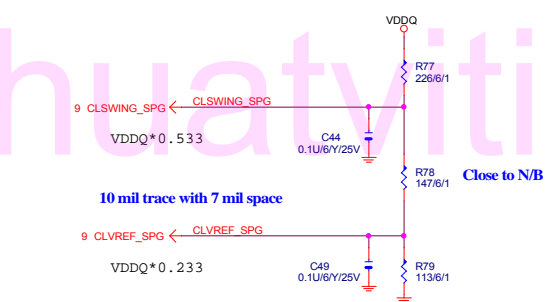
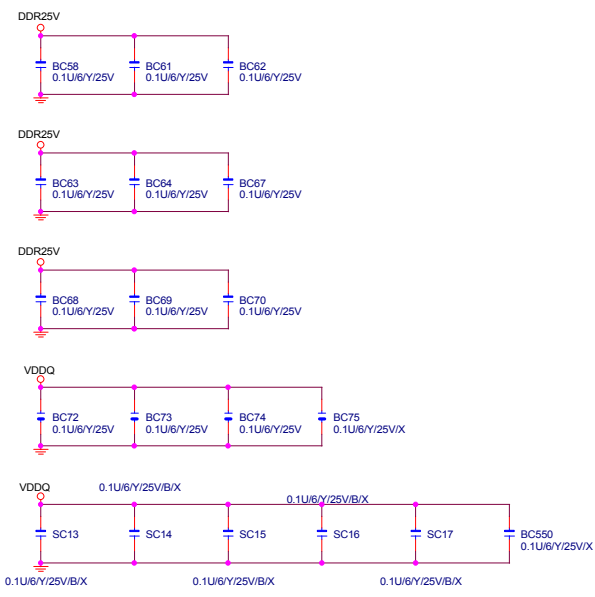
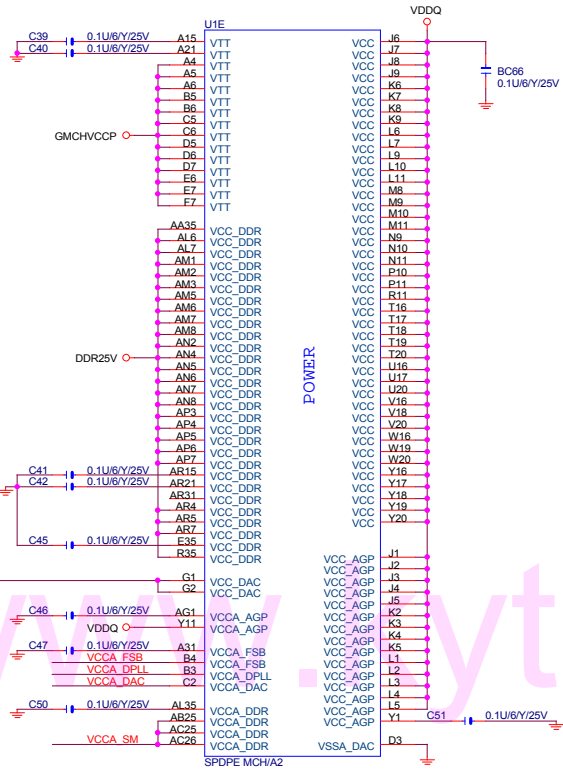
DDR 400 1-2-3-4 CPC DISABLE
 DDR 333 SIGNAL 1 CPC ENABLE
 2 CPC DISABLE
 DUAL 2 CPC ENABLE
 DUAL 4 CPC DISABLE



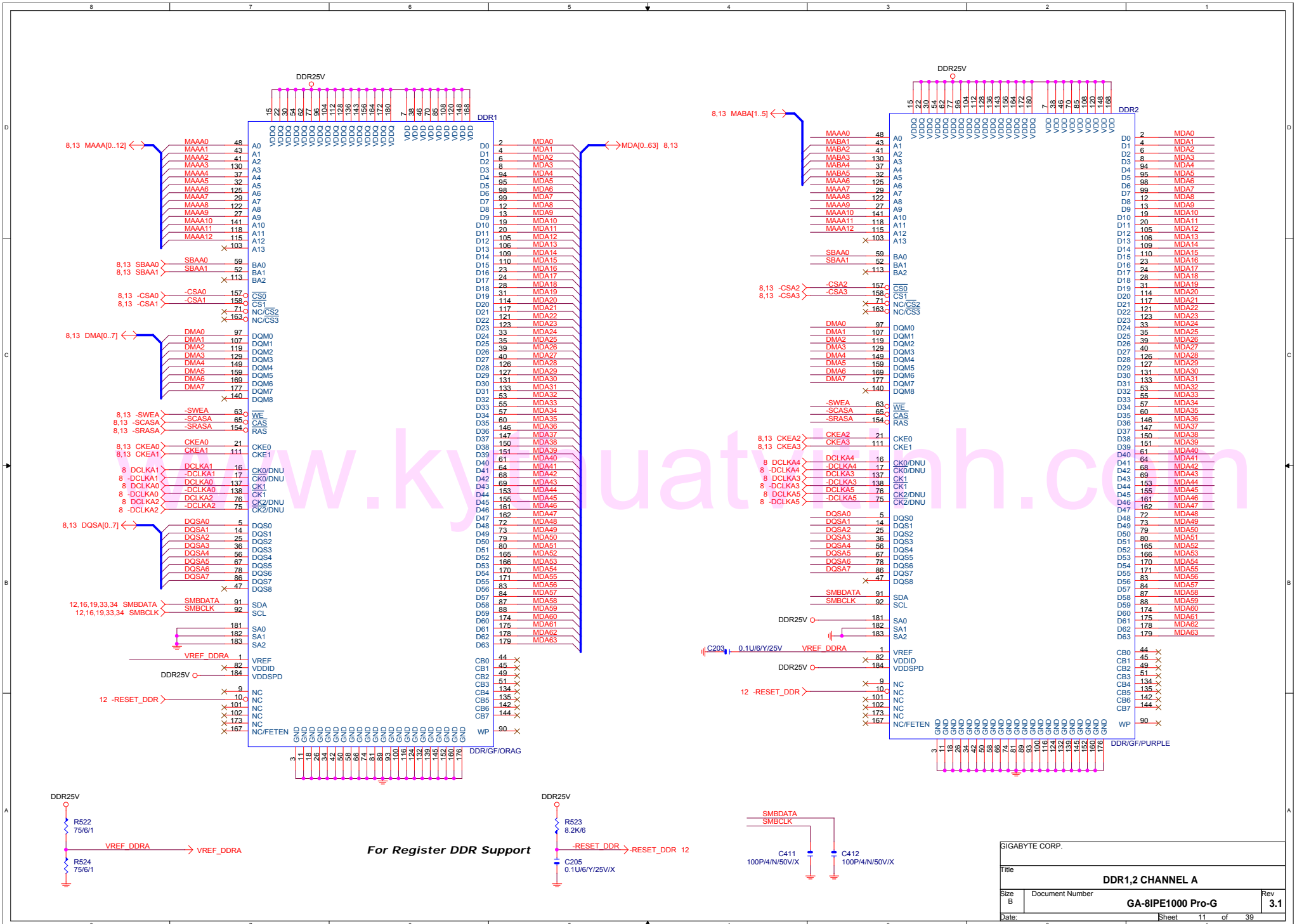
14 GAD[0..31] <-> GAD[0..31]
 14 SBA[0..7] <-> SBA[0..7]
 15 HL[0..10] <-> HL[0..10]



Title		
SPRINGDALE AGP,HUB,CSA,VGA		
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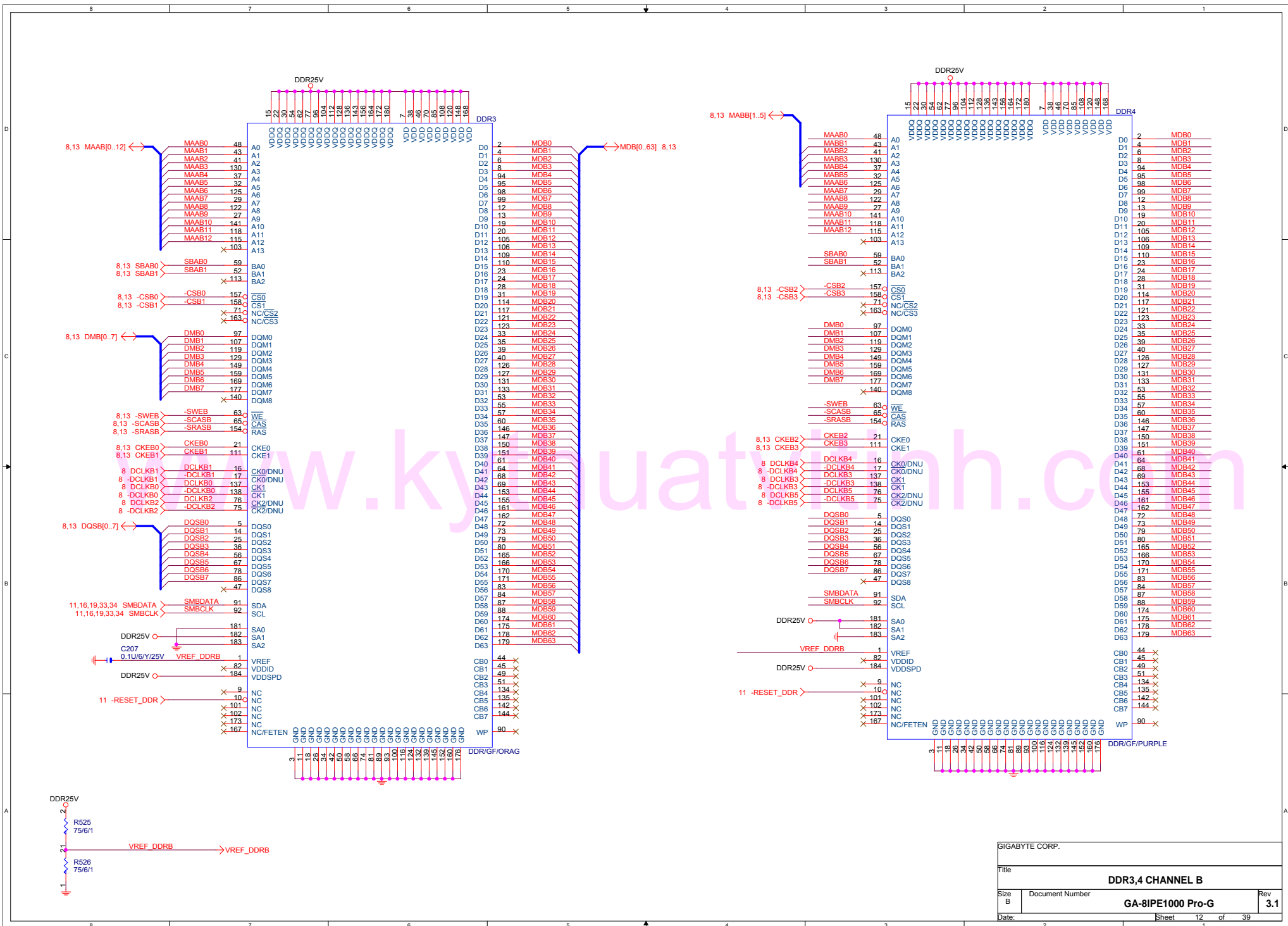


Title			
SPRINGDALE PWR			
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For Register DDR Support

SIGABYTE CORP.		
Title		
DDR1,2 CHANNEL A		
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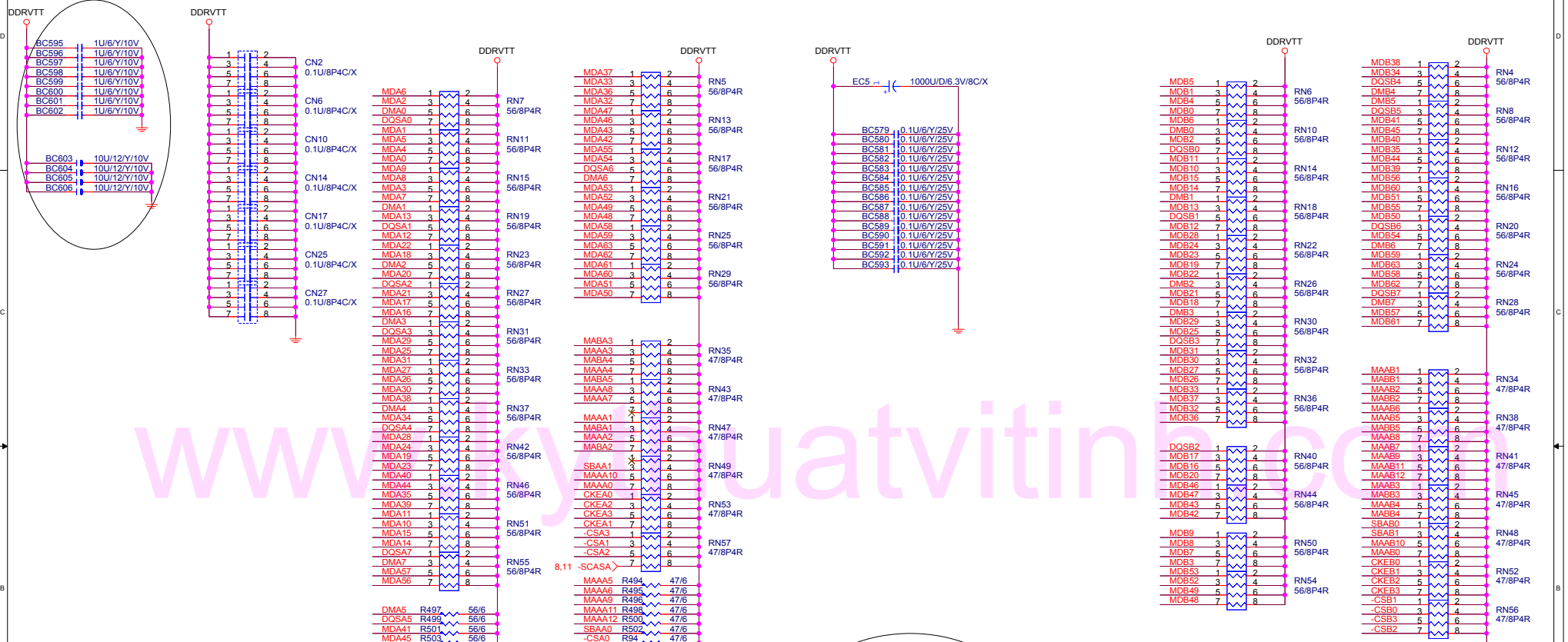


DDRVTT Decouple

DDR TERMINATION CHANNEL A

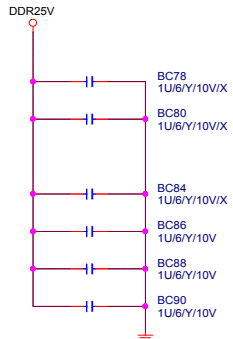
DDRVTT Decouple

CHANNEL B



DDR25V Decouple

DDR25V Decouple

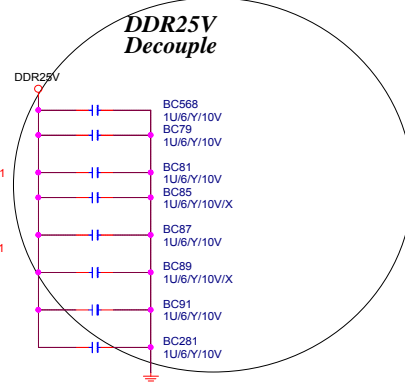


47 Ohms

- SBA0[0..1] <- SBA[0..1] 8,11
- CSA[0..3] <- CSA[0..3] 8,11
- CKEA[0..3] <- CKEA[0..3] 8,11
- MABA[1..5] <- MABA[1..5] 8,11
- MAAA[0..12] <- MAAA[0..12] 8,11

56 Ohms

- DQSA[0..7] <- DQSA[0..7] 8,11
- DMA[0..7] <- DMA[0..7] 8,11
- MDA[0..63] <- MDA[0..63] 8,11



47 Ohms

- SBAB[0..11] <- SBAB[0..11] 8,12
- CSB[0..3] <- CSB[0..3] 8,12
- CKEB[0..3] <- CKEB[0..3] 8,12
- MABB[1..5] <- MABB[1..5] 8,12
- MAAB[0..12] <- MAAB[0..12] 8,12

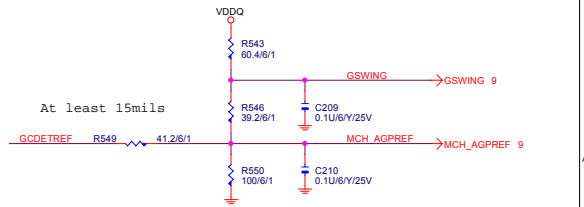
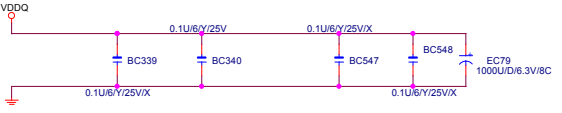
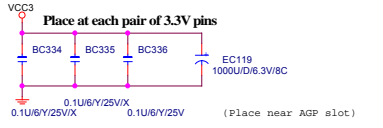
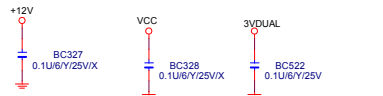
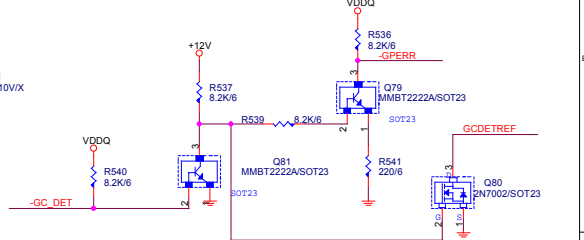
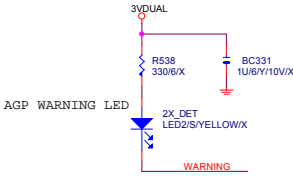
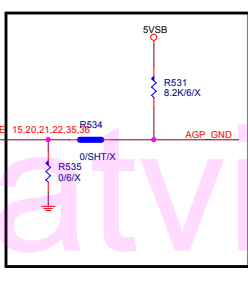
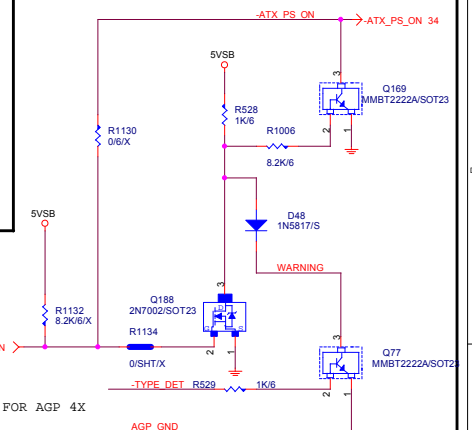
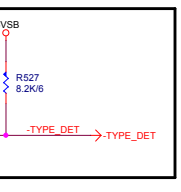
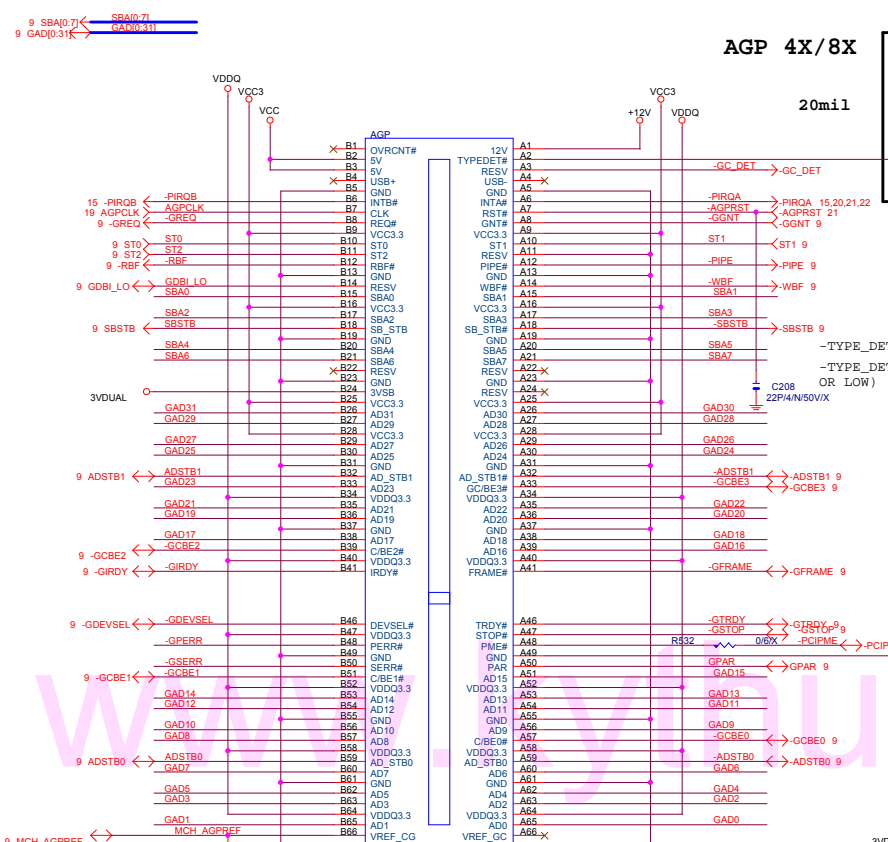
56 Ohms

- DQSB[0..7] <- DQSB[0..7] 8,12
- DMB[0..7] <- DMB[0..7] 8,12
- MDB[0..63] <- MDB[0..63] 8,12

SIGABYTE CORP.		
Title		
DDR TERMINATION		
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AGP 4X/8X

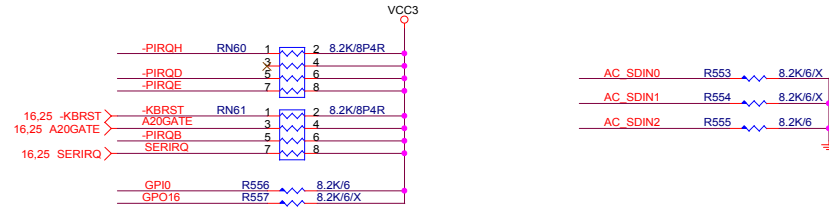
20mil



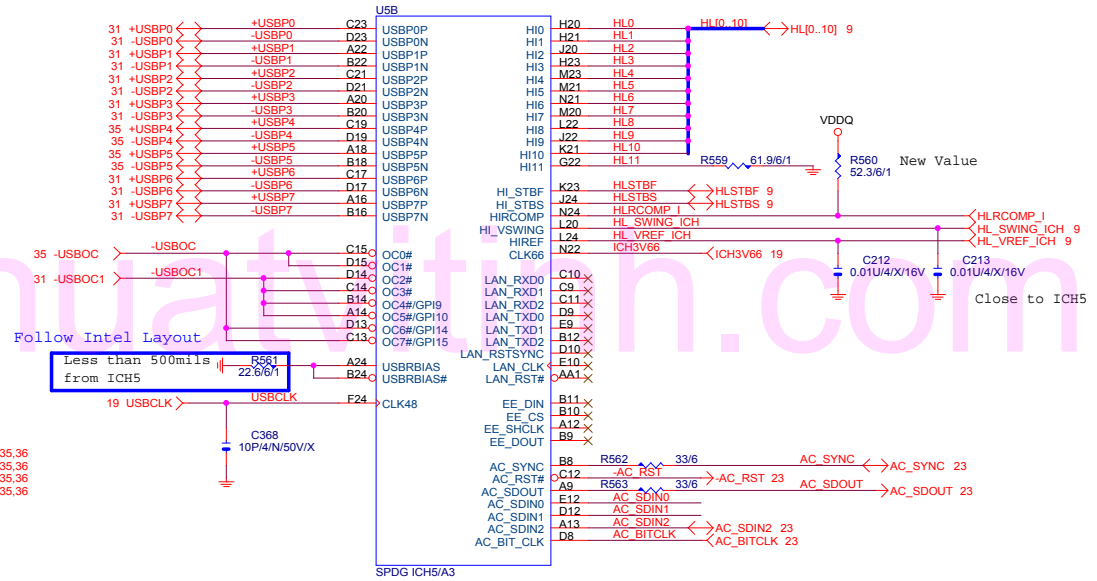
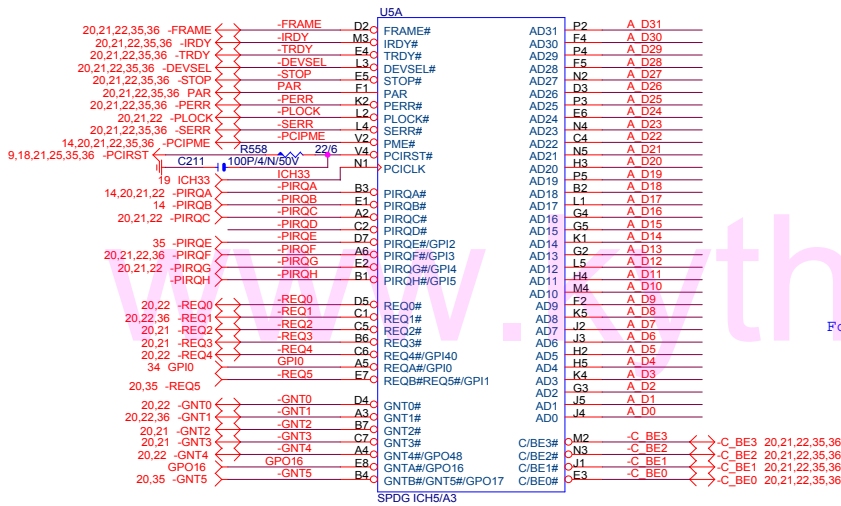
Place 1 at each pair of VDDQ pins
Place an additional for spread from A14 - A33

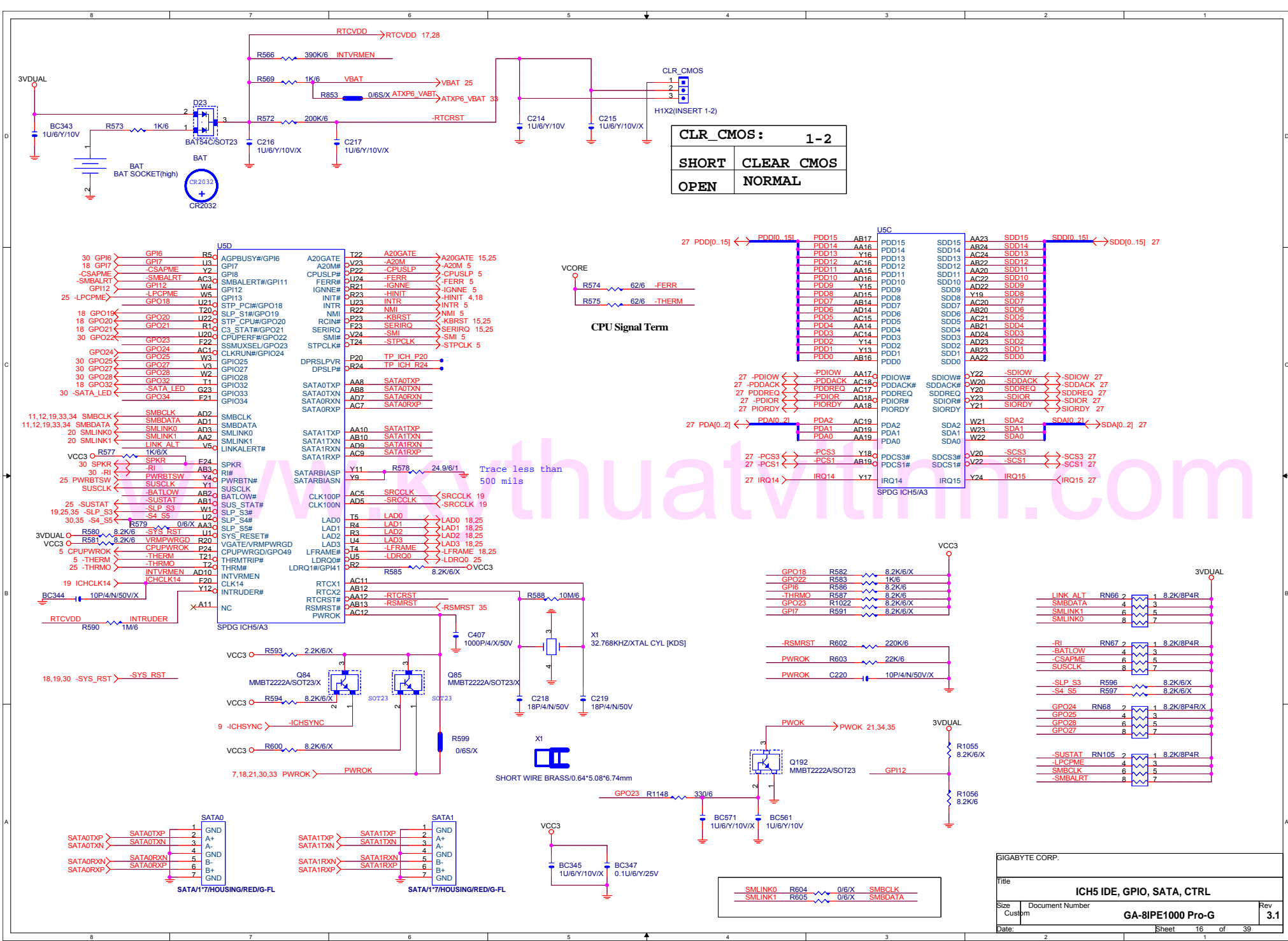
GIGABYTE CORP.

Title			AGP SLOT		
Customer			GA-8IPE1000 Pro-G		
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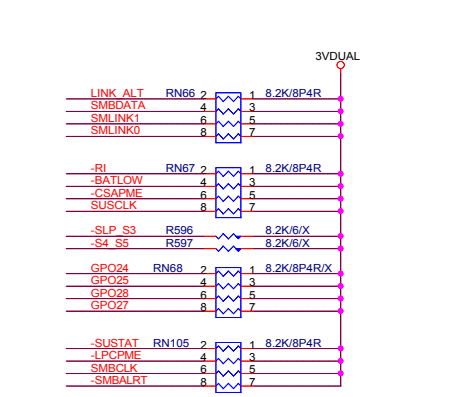
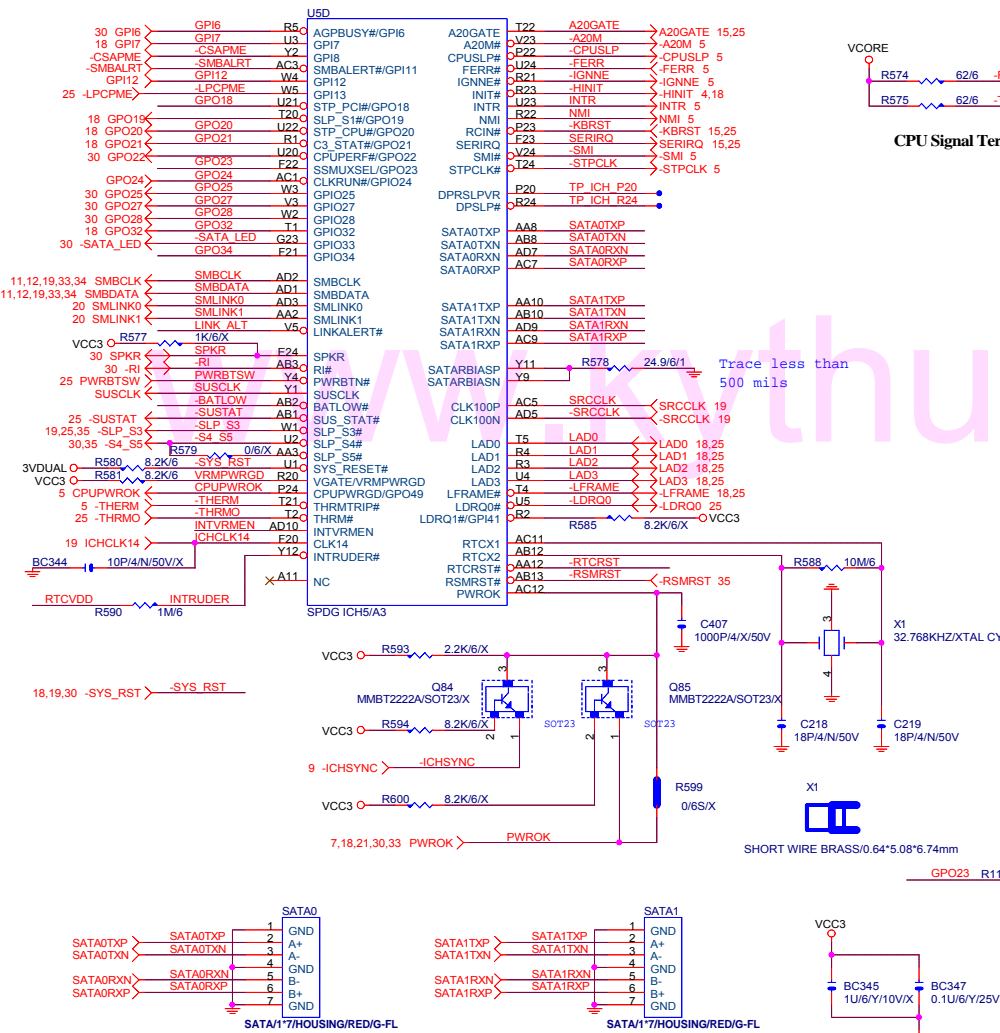
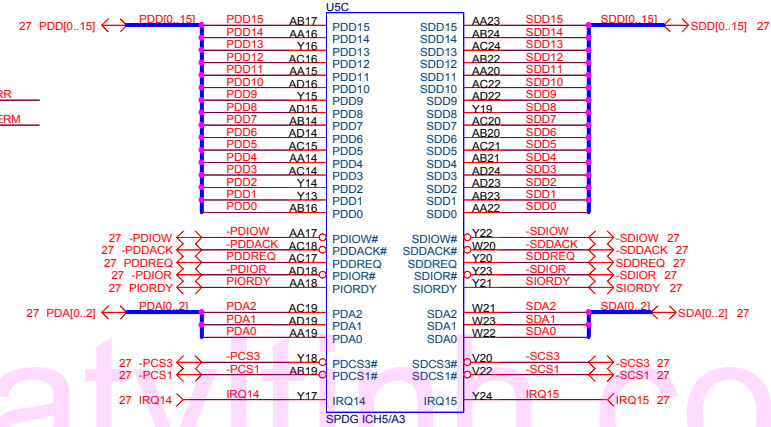


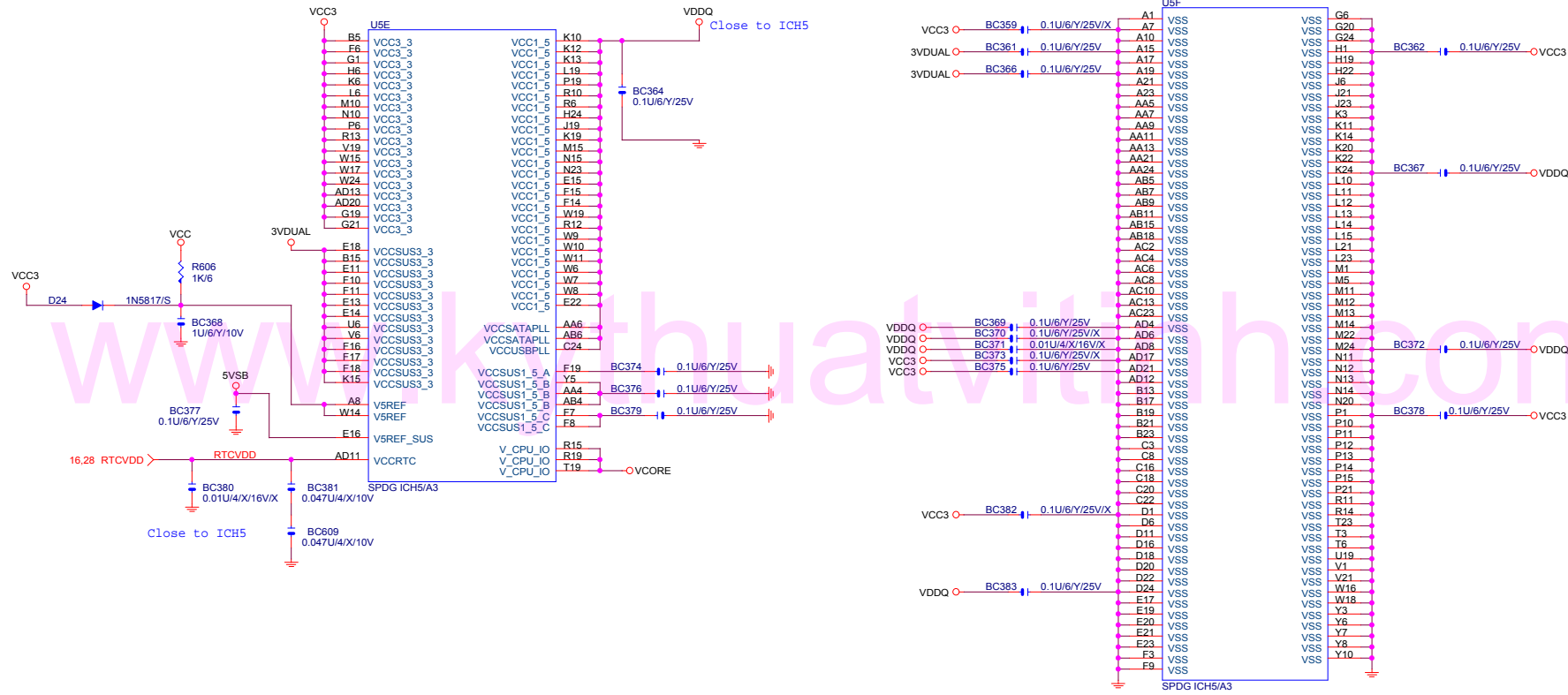
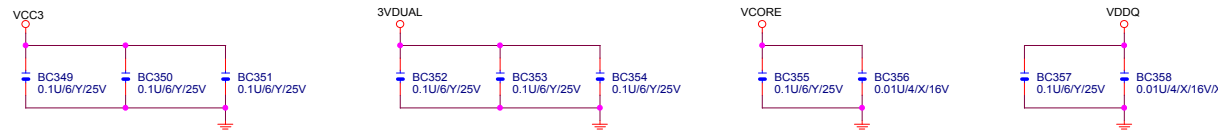
A_D0_311 <-> A_D0[.31] 20,21,22,35,36

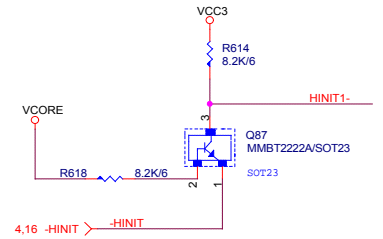
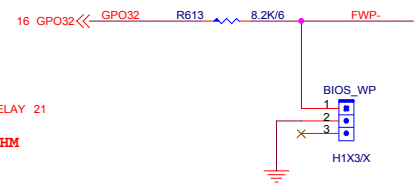
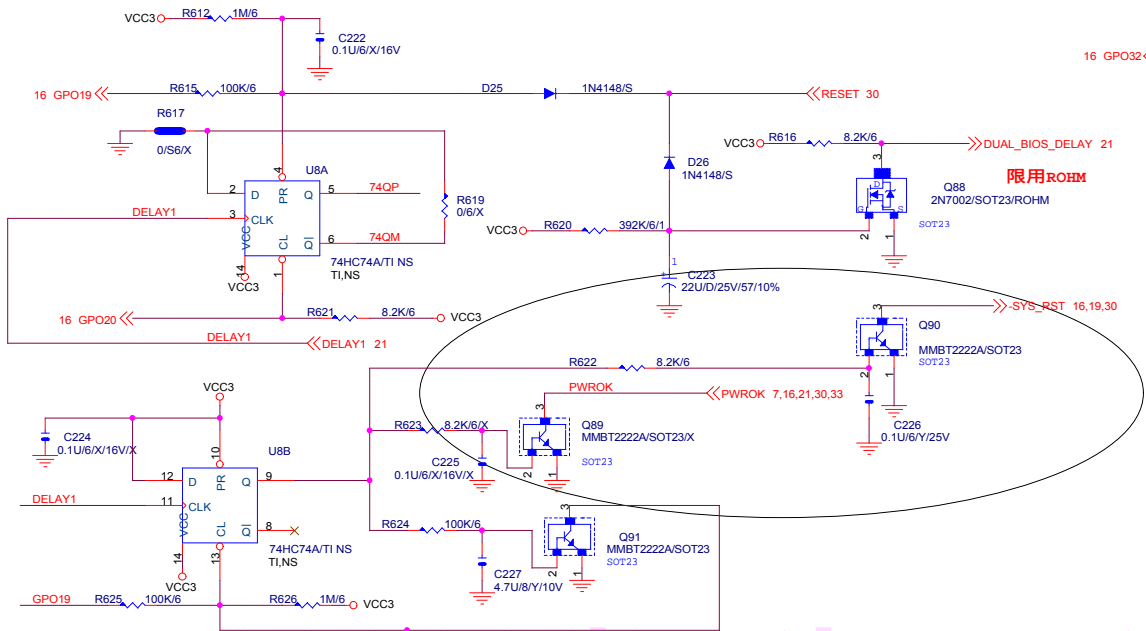




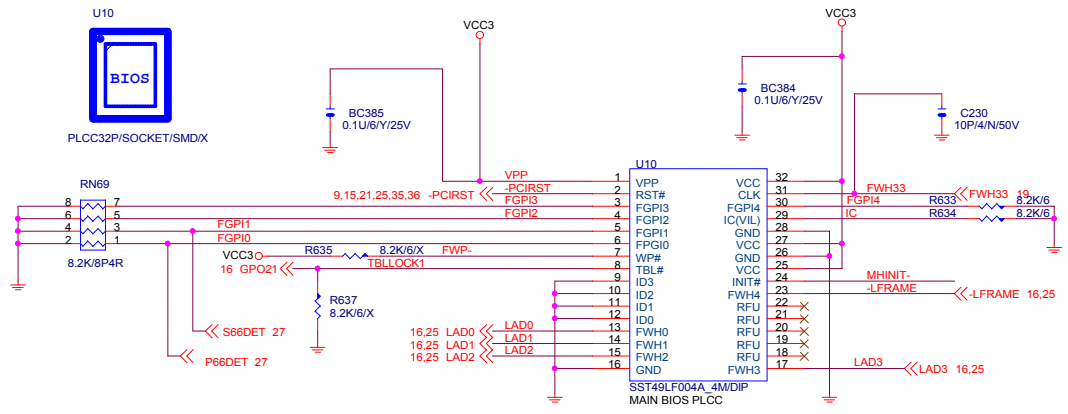
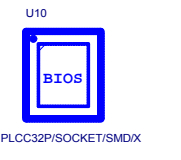
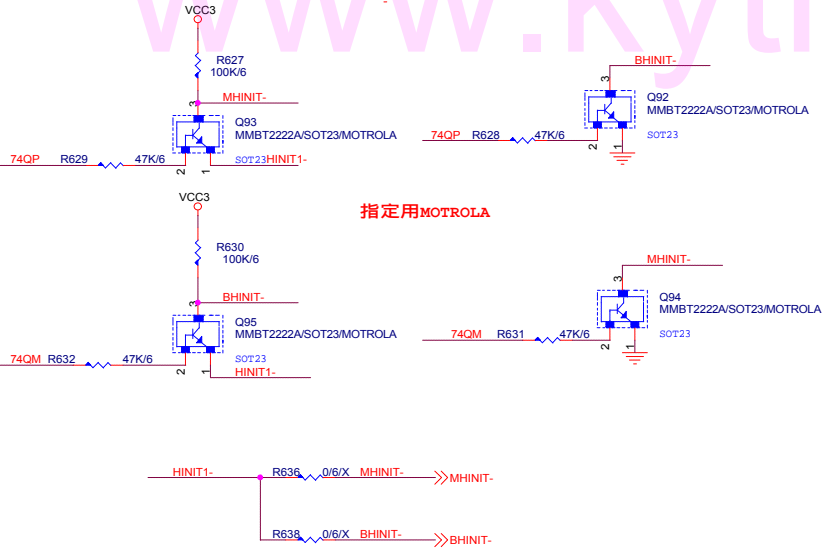
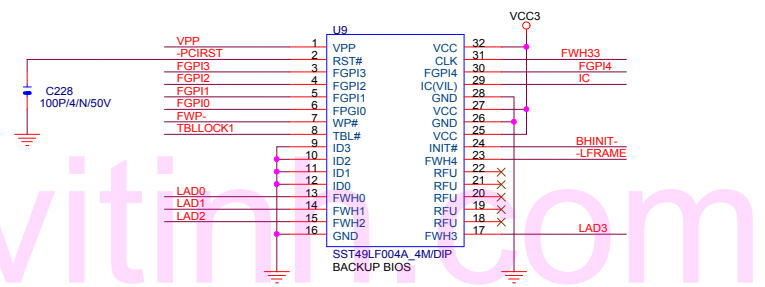
CLR_CMOS :	
SHORT	CLEAR CMOS
OPEN	NORMAL





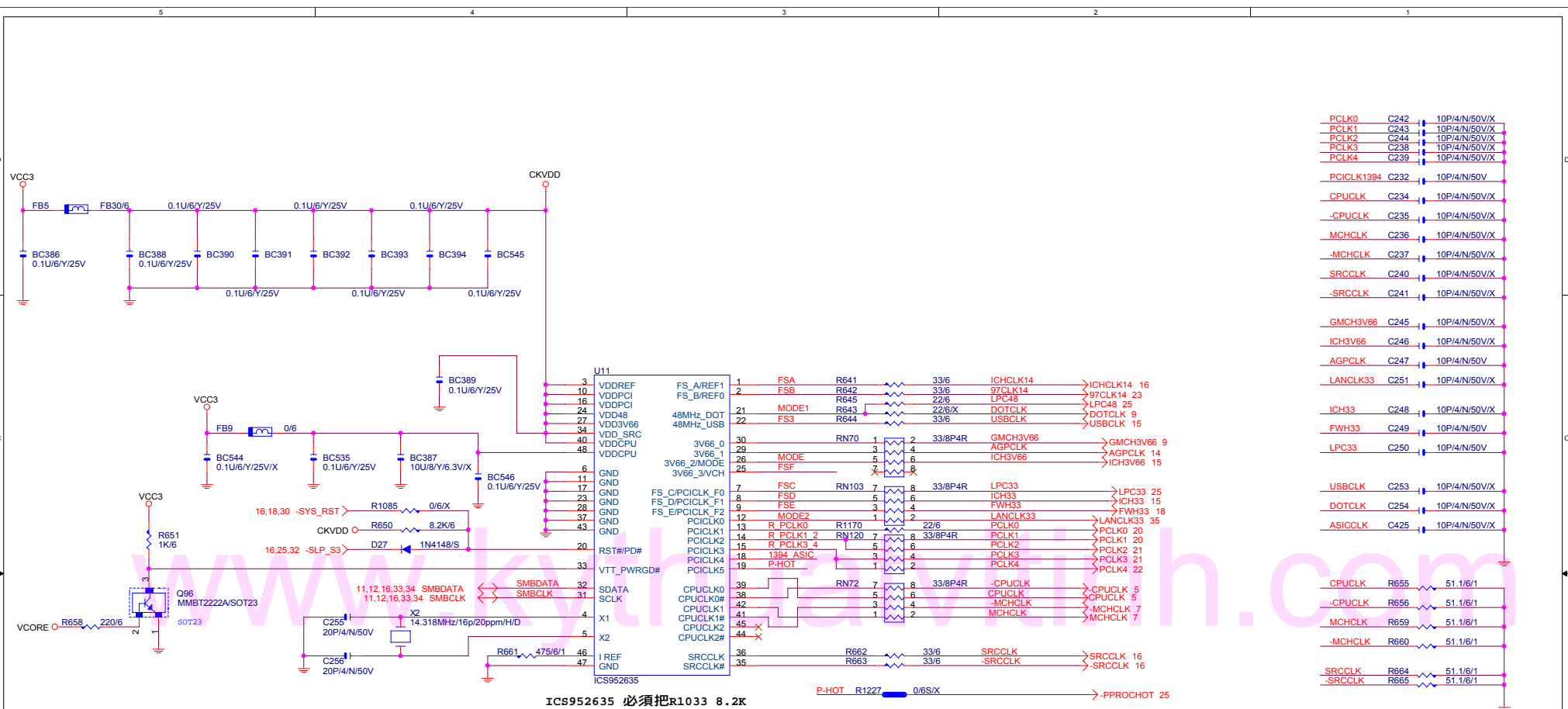


BIOS_WP:	
1-2	WRITE PROTECT
2-3	DISABLE



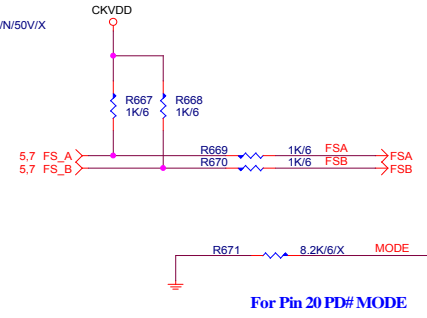
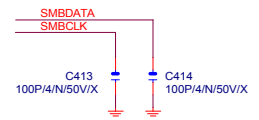
SIGABYTE CORP.		
Title		
FWH		
Size	Document Number	Rev
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ADD WINBOUD FWH SEC. SOURCE



- PCLK0 C242 10P/4/N/50V/X
- PCLK1 C243 10P/4/N/50V/X
- PCLK2 C244 10P/4/N/50V/X
- PCLK3 C238 10P/4/N/50V/X
- PCLK4 C239 10P/4/N/50V/X
- PCICKL1394 C232 10P/4/N/50V
- CPUCCLK C234 10P/4/N/50V/X
- CPUCCLK C235 10P/4/N/50V/X
- MCHCLK C236 10P/4/N/50V/X
- MCHCLK C237 10P/4/N/50V/X
- SRCCCLK C240 10P/4/N/50V/X
- SRCCCLK C241 10P/4/N/50V/X
- GMCH3V66 C245 10P/4/N/50V/X
- ICH3V66 C246 10P/4/N/50V/X
- AGPCLK C247 10P/4/N/50V
- LANCLK33 C251 10P/4/N/50V/X
- ICH33 C248 10P/4/N/50V/X
- FWH33 C249 10P/4/N/50V
- LPC33 C250 10P/4/N/50V
- USBCLK C253 10P/4/N/50V/X
- DOTCLK C254 10P/4/N/50V/X
- ASICCLK C425 10P/4/N/50V/X
- CPUCCLK R655 51.1/6/1
- CPUCCLK R656 51.1/6/1
- MCHCLK R659 51.1/6/1
- MCHCLK R660 51.1/6/1
- SRCCCLK R664 51.1/6/1
- SRCCCLK R665 51.1/6/1

ICS952635 必須把R1033 8.2K REMOVE



For Pin 20 PD# MODE

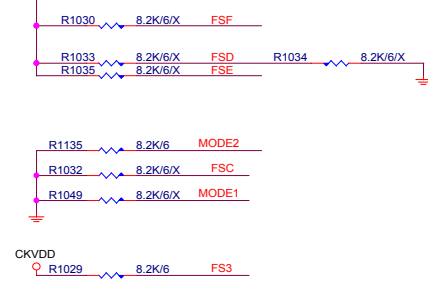
CYPRESS CY28405

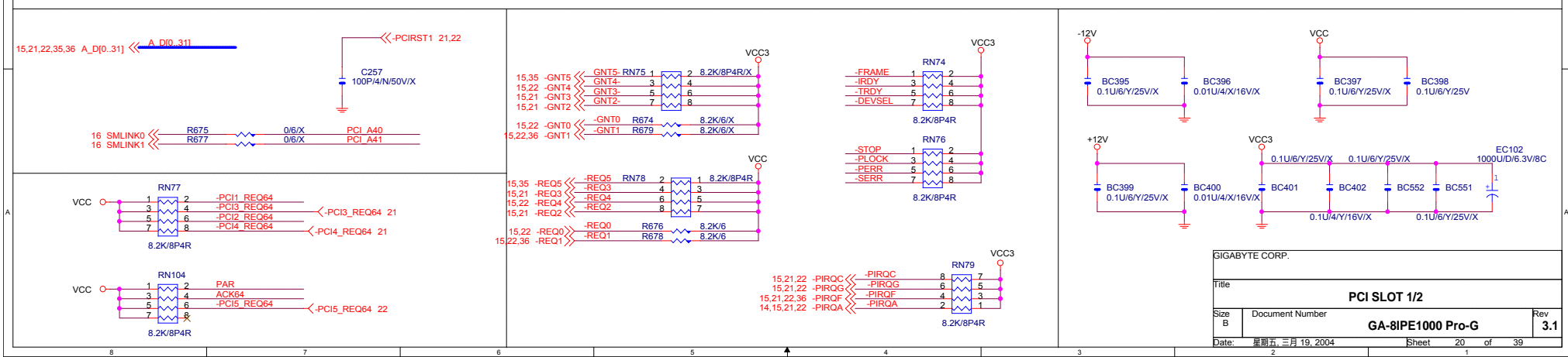
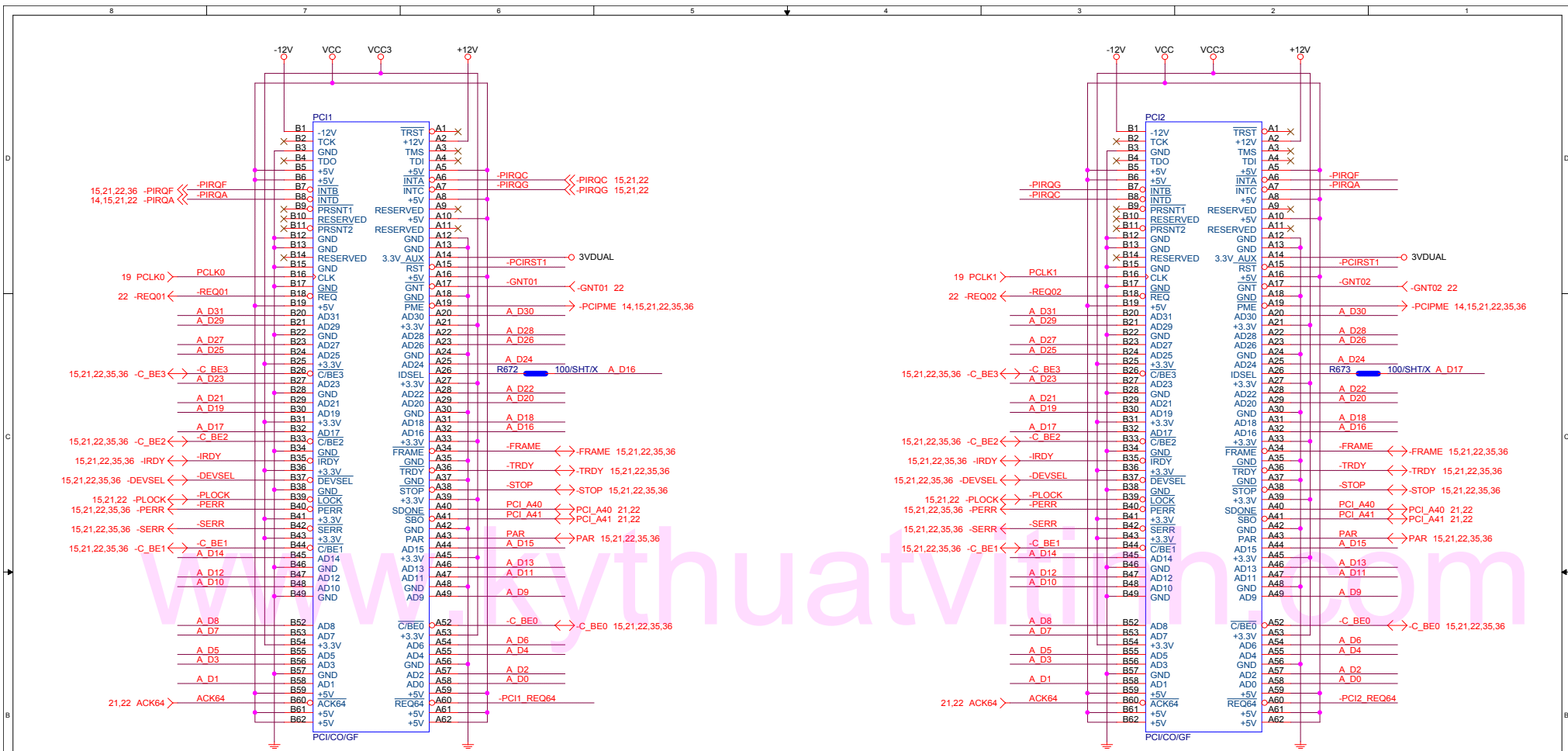
FS_E	FS_D	FS_C	FS_B	FS_A	Clock
1	1	0	0	0	100.9MHz
1	1	0	0	1	133.9MHz
1	1	0	1	1	166.9MHz
1	1	0	1	0	200.9MHz

ICS952616

FS_E	FS_3	FS_C	FS_B	FS_A	Clock
1	0	0	0	0	100MHz
1	0	0	0	1	133MHz
1	0	0	1	1	166MHz
1	0	0	1	0	200MHz

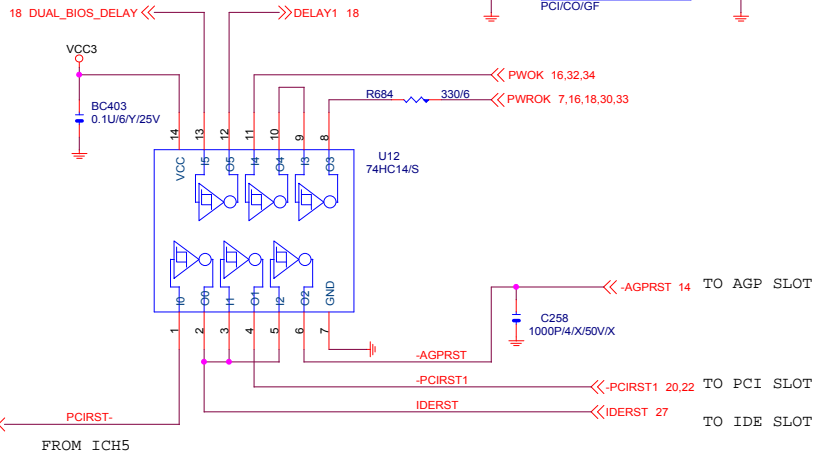
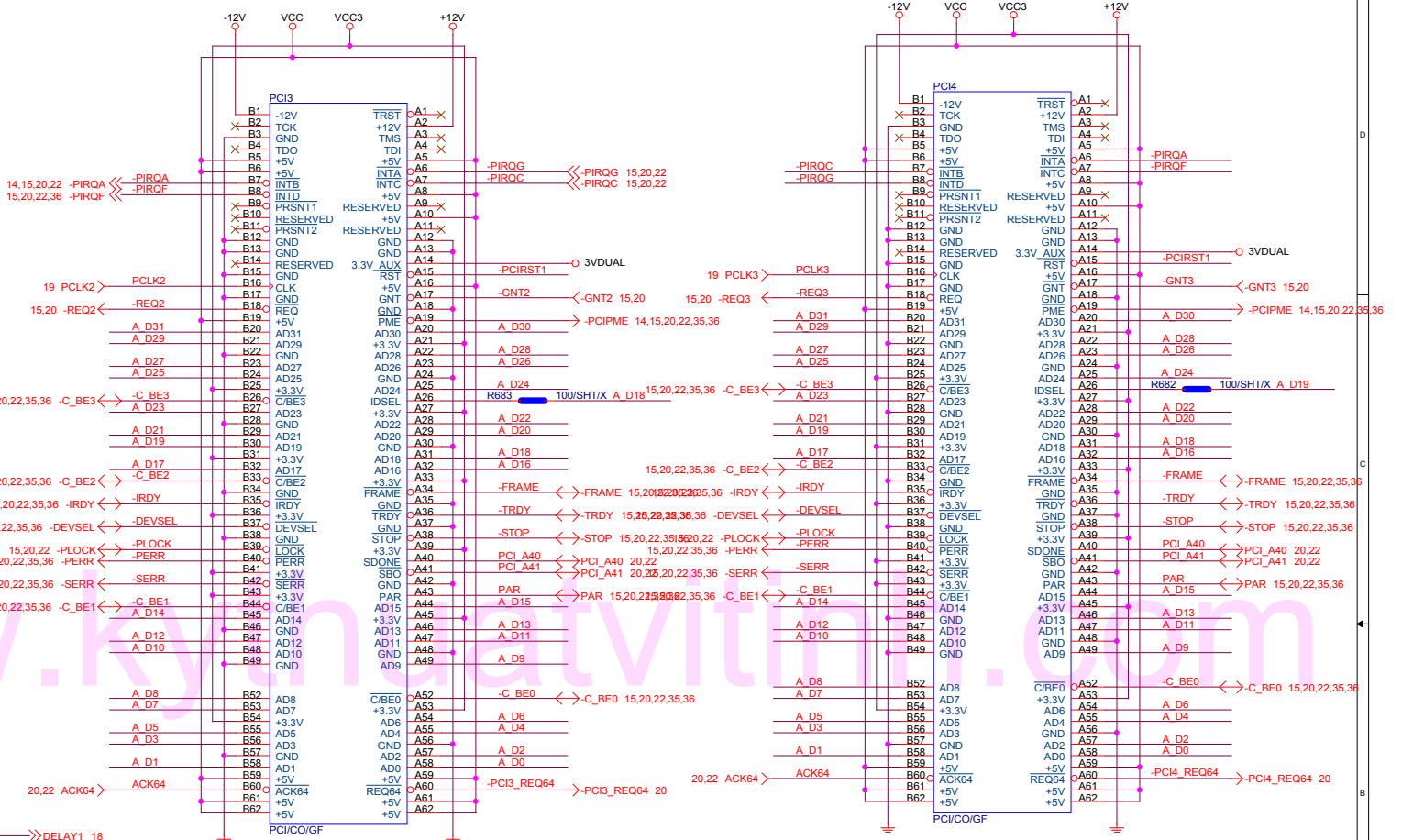
ICS + CYPRESS CO-LAYOUT





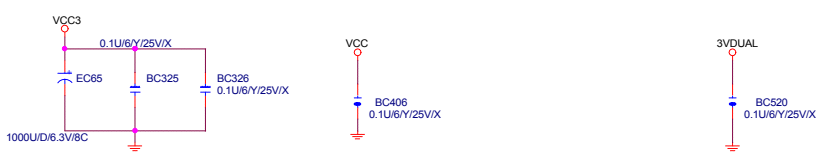
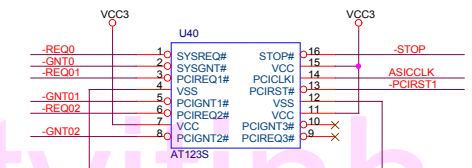
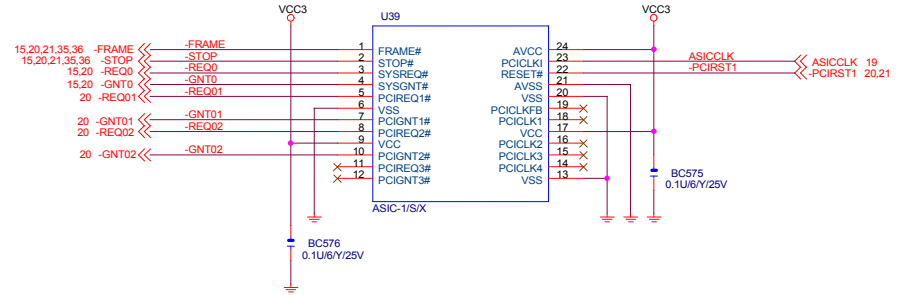
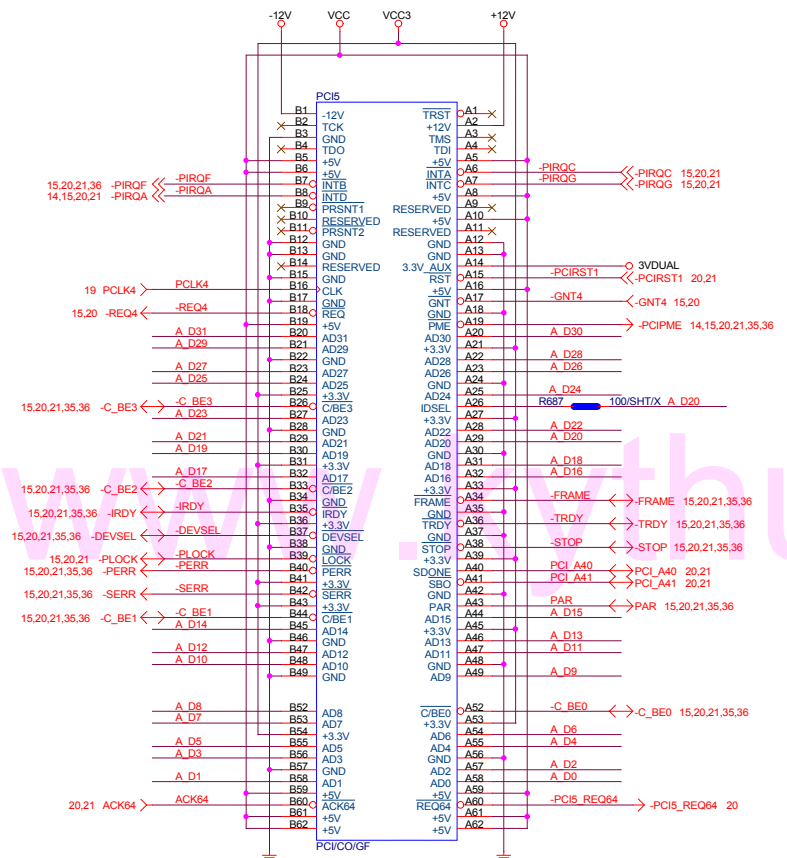
GIGABYTE CORP.		
Title		
PCI SLOT 1/2		
Size	Document Number	Rev
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15,20,22,35,36 A_D[0..31] << A_D[0..31]



GIGABYTE CORP.		
Title PCI SLOT 3/4		
Size B	Document Number GA-8IPE1000 Pro-G	Rev 3.1
Date 星期五, 三月 19, 2004	Sheet 21	of 39

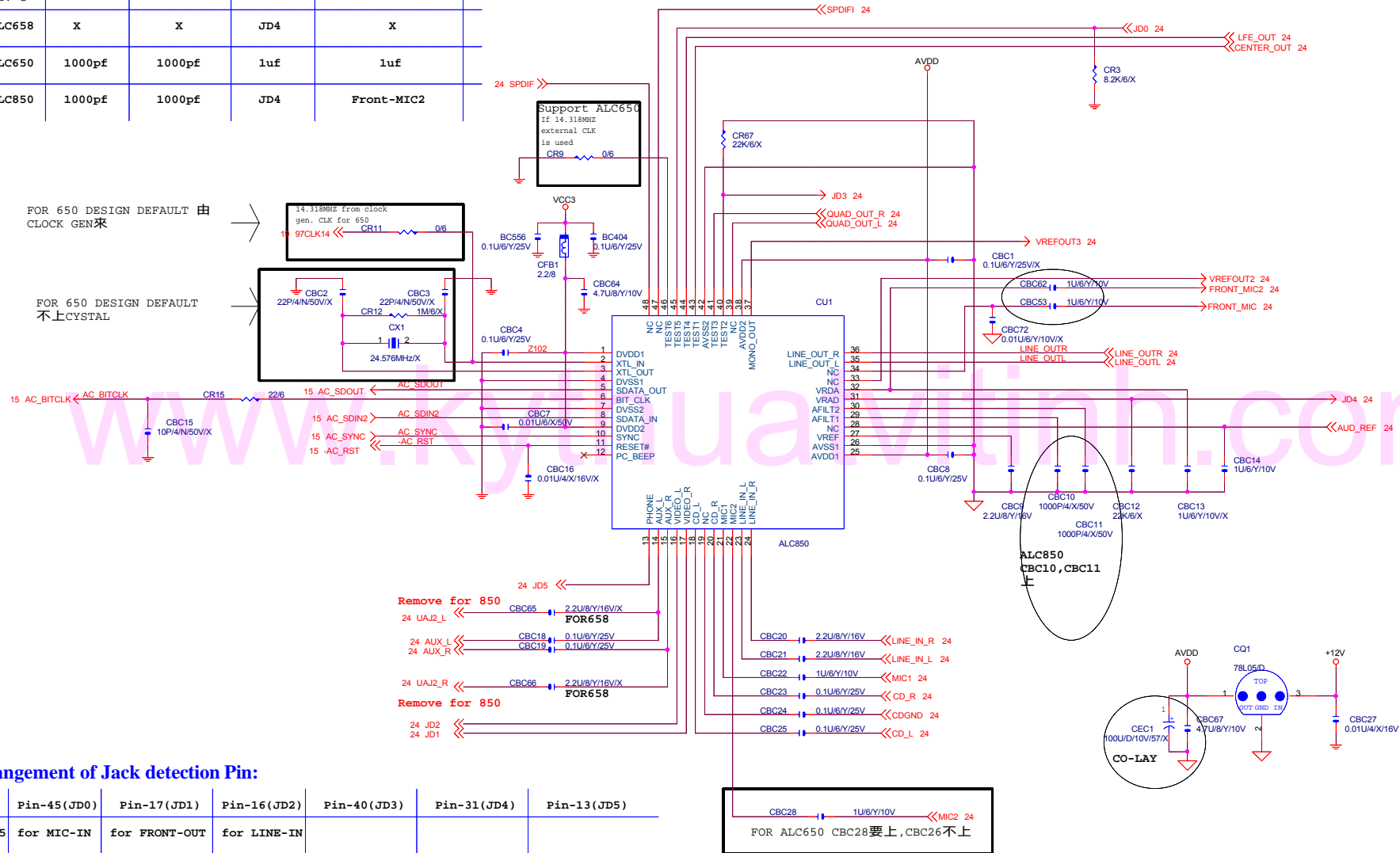
15,20,21,35,36_A_D[0..31] << A_D[0..31]



GIGABYTE CORP.			
Title			
PCI SLOT 5			
Size	Document Number	Rev	
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Filter Cap design:

	Pin-29	Pin-30	Pin-31	Pin-32
ALC655 Rev D	1000pf	1000pf	1uf	Front-MIC2
ALC655 Rev C	1000pf	1000pf	1uf	X
ALC658	X	X	JD4	X
ALC650	1000pf	1000pf	1uf	1uf
ALC850	1000pf	1000pf	JD4	Front-MIC2

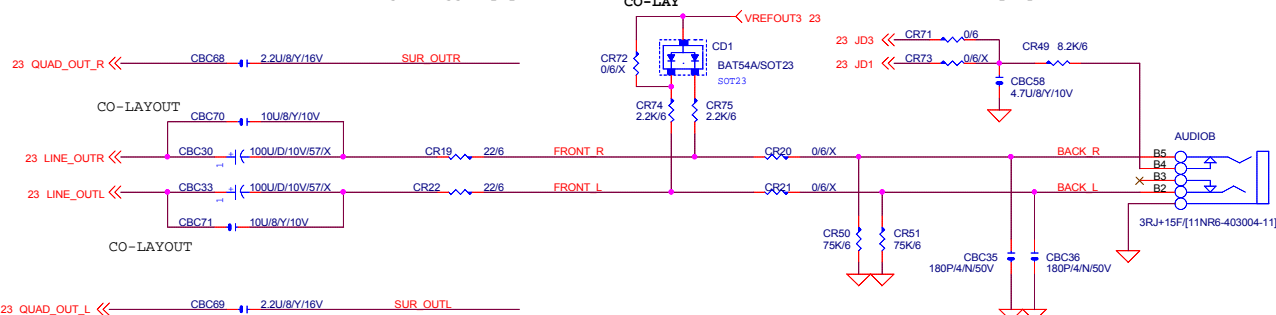


Arrangement of Jack detection Pin:

	Pin-45(JD0)	Pin-17(JD1)	Pin-16(JD2)	Pin-40(JD3)	Pin-31(JD4)	Pin-13(JD5)
ALC655	for MIC-IN	for FRONT-OUT	for LINE-IN			
ALC658	for MIC-IN	for UAJ1	for UAJ2	for FRONT-OUT External pull high is needed	for LINE-IN External pull high is needed	
ALC850	for MIC-IN	for Front Pannel OUT	for Front Pannel IN	for FRONT-OUT	for LINE-IN	for SurrBack Out

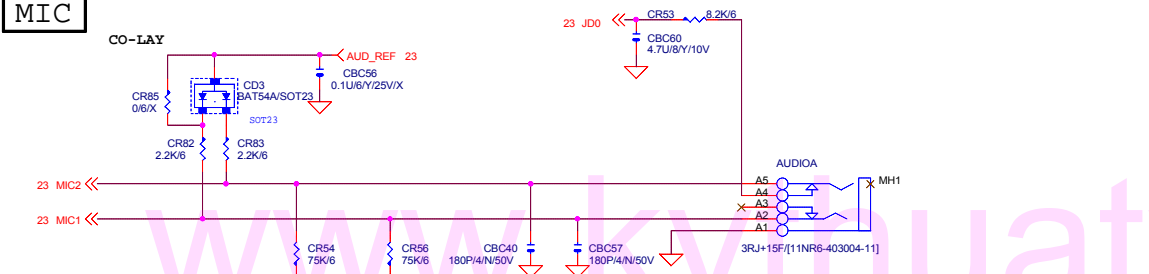
LINE OUT

JDO,JD2,GPIO0 為偵測DEVICE INPUT 時由LOW TO HIGH Edge trigger(pop manual) 1/2(3.14)RC=1/2(3.14)8.2K*4.7U=4.3HZ以上AC 信號全部衰減 TO 0V 不會造成JDO 誤動作(無device 時play wav)



LINE OUT SENSING
 R>4K OHM=>POWER SPEAKER
 4K OHM>R>400 OHM=>MICROPHONE
 R<400 OHM=>HEADPHONE

MIC



MICROPHONE IN SENSING(當INPUT) (利用vref 偏壓 與CR43,CR32 並聯求出阻抗)
 7.1k ohm>R>2.3k ohm==>microphone in
 R<2.3k ohm or R>7.1k ohm==>unknown device

MICROPHONE IN SENSING(當OUTPUT)
 R>4K OHM=>POWER SPEAKER
 4K OHM>R>400 OHM=>MICROPHONE
 R<400 OHM=>HEADPHONE

2x5 header for 850

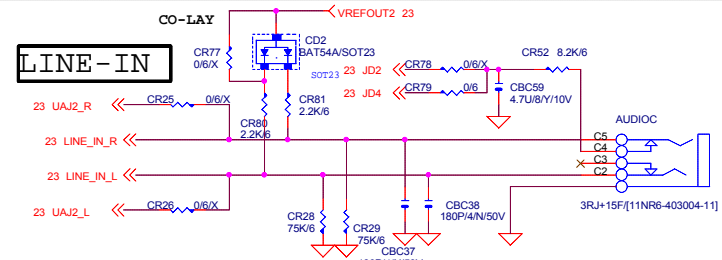
For 850 if JD5 = low AUX-In is configured as input
 For 850 if JD5 = high AUX-In is configured as output, Surr-Back out

For 850 AUX-In is shared to Surr-Back out

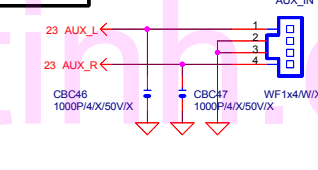
LINE IN SENSING(當OUTPUT)
 R>4K OHM=>POWER SPEAKER
 4K OHM>R>400 OHM=>MICROPHONE
 R<400 OHM=>HEADPHONE

LINE IN SENSING(當INPUT)
 swing of input signal>-40dbv(10mv)==>line in device active
 swing of input signal<-40dbv(10mv)==>unknown line in device

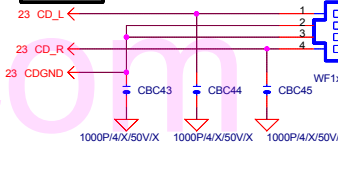
LINE-IN



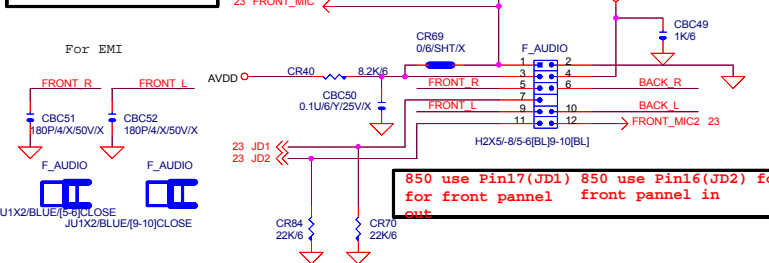
AUX IN DEFAULT NO POP



CD IN

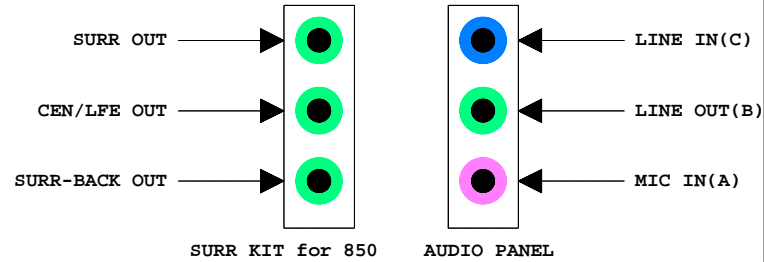
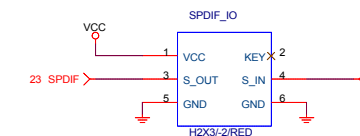


INTEL FRONT AUDIO



850 use Pin17(JD1) 850 use Pin16(JD2) for front panel front panel in out

SPDIF_IO



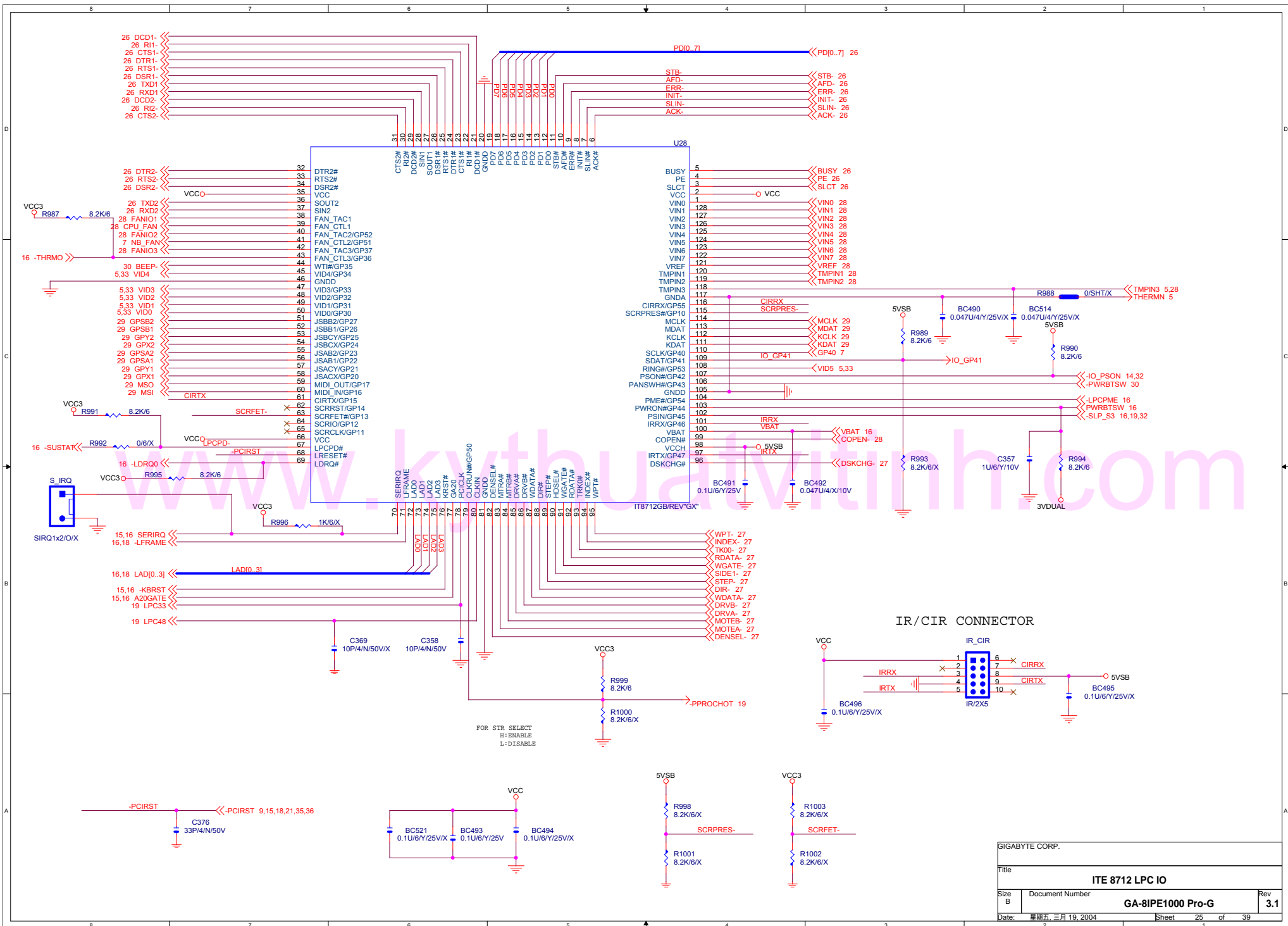
SURR KIT for 850

AUDIO PANEL

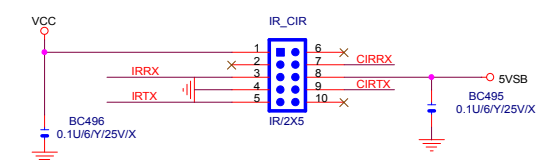
GIGABYTE CORP.

AUDIO OUTPUT, GAME PORT

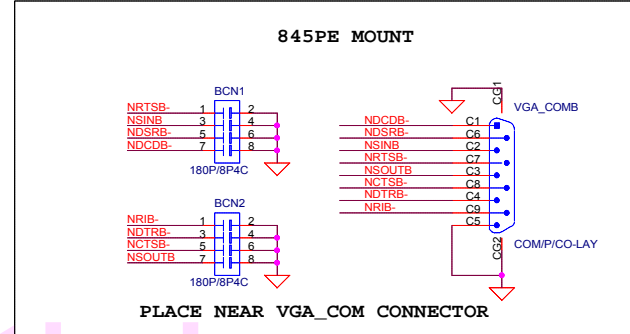
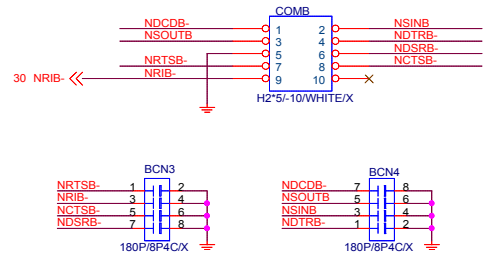
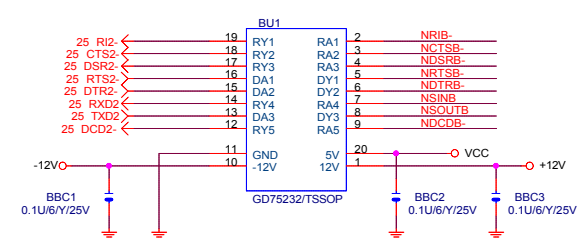
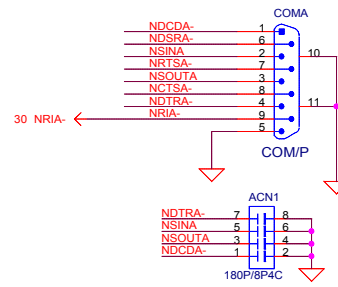
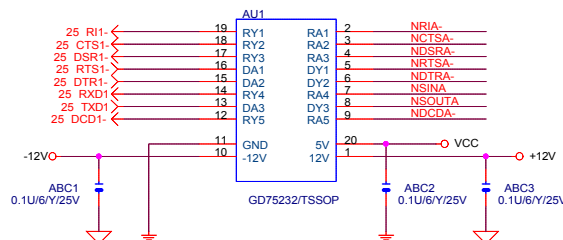
Title	Document Number		Rev
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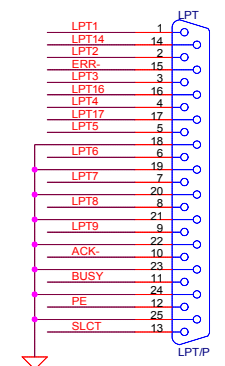
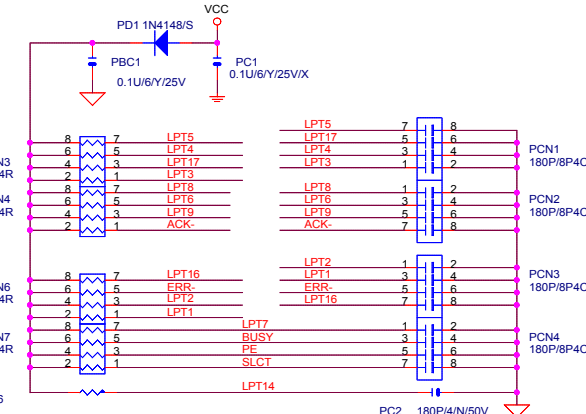
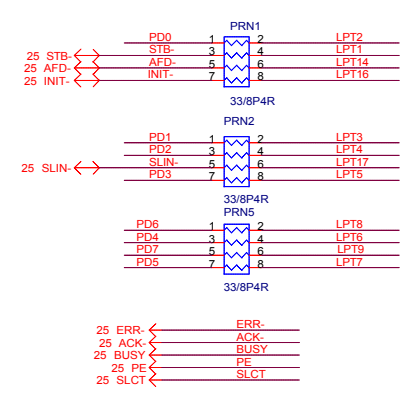
IR/CIR CONNECTOR

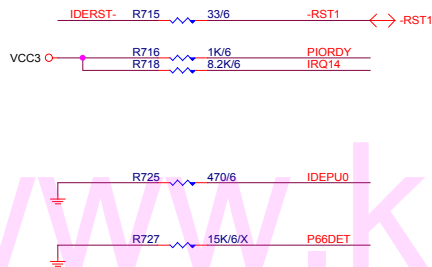
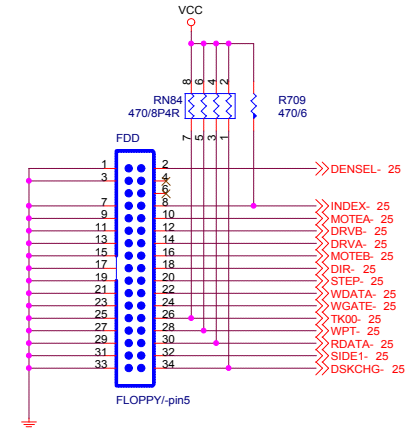
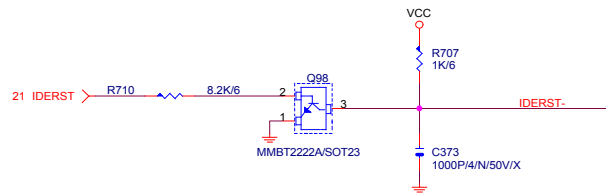


SIGABYTE CORP.		
Title		
ITE 8712 LPC IO		
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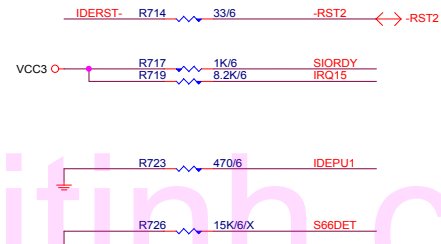


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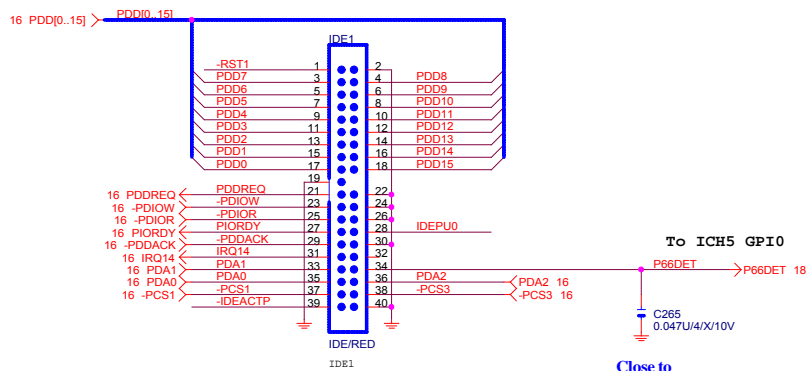




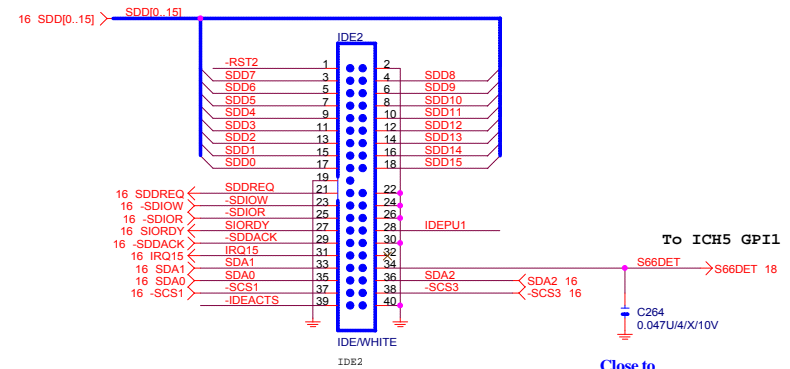
PRIMARY IDE CONNECTOR



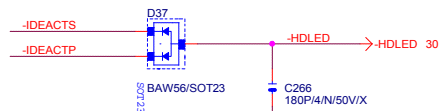
SECONDARY IDE CONNECTOR



Close to connector



Close to connector



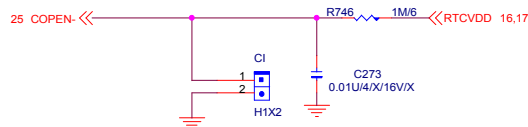
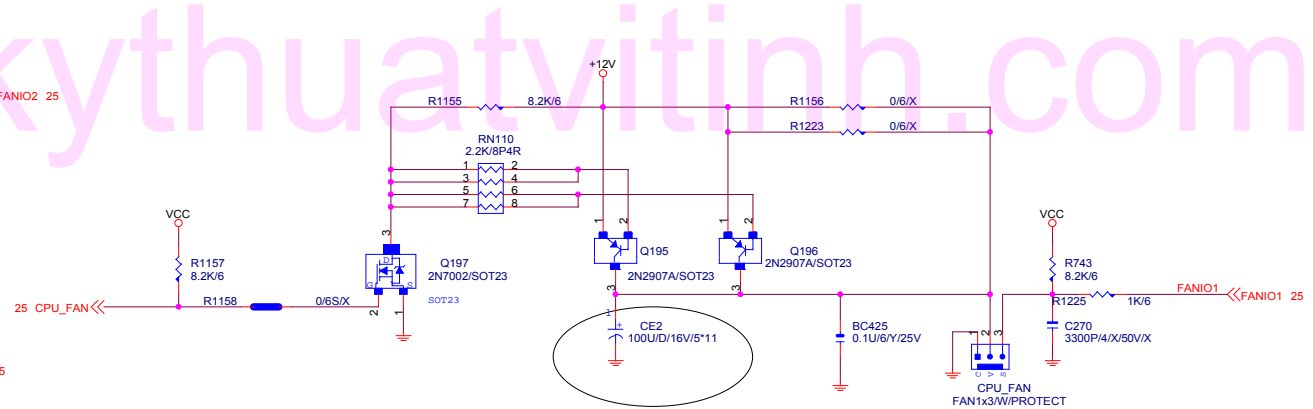
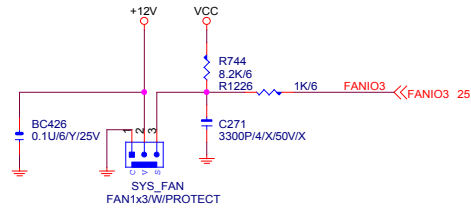
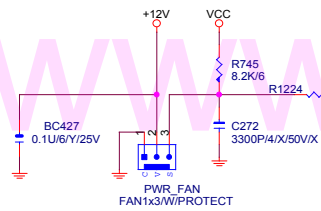
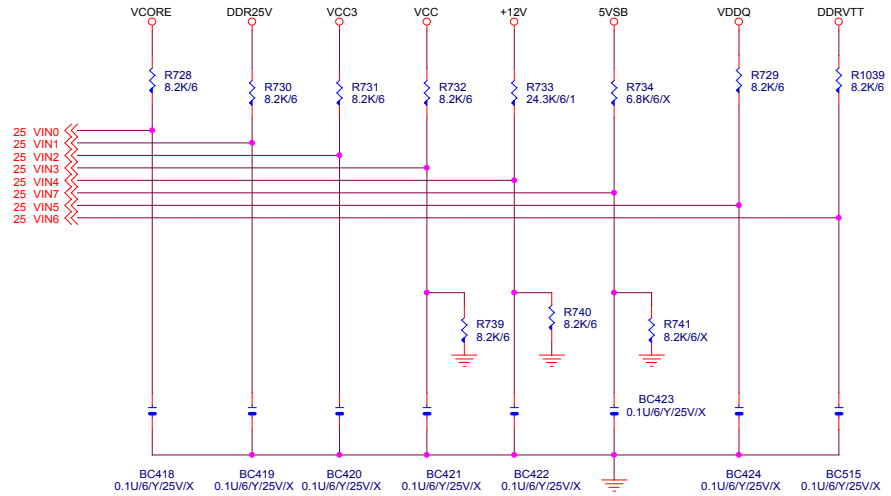
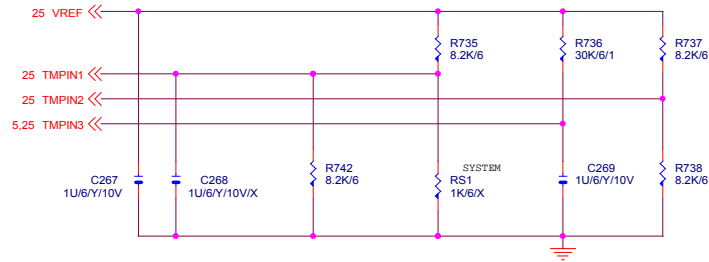
GIGABYTE CORP.

Title
IDE CONNECTOR

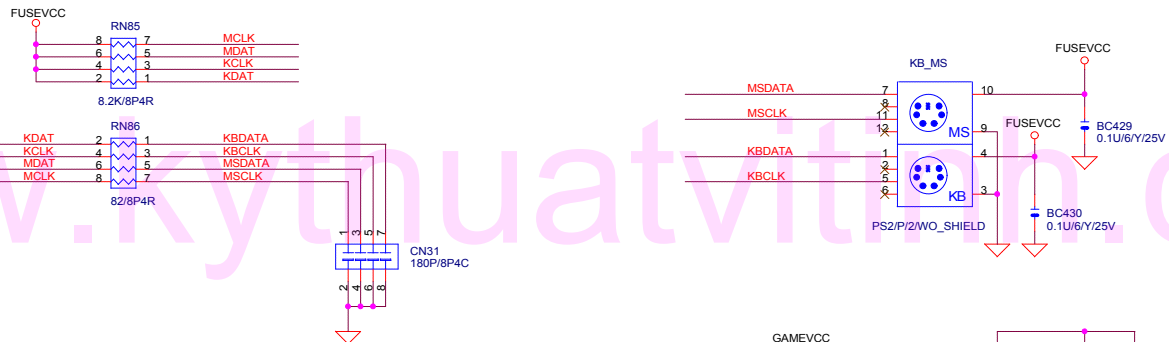
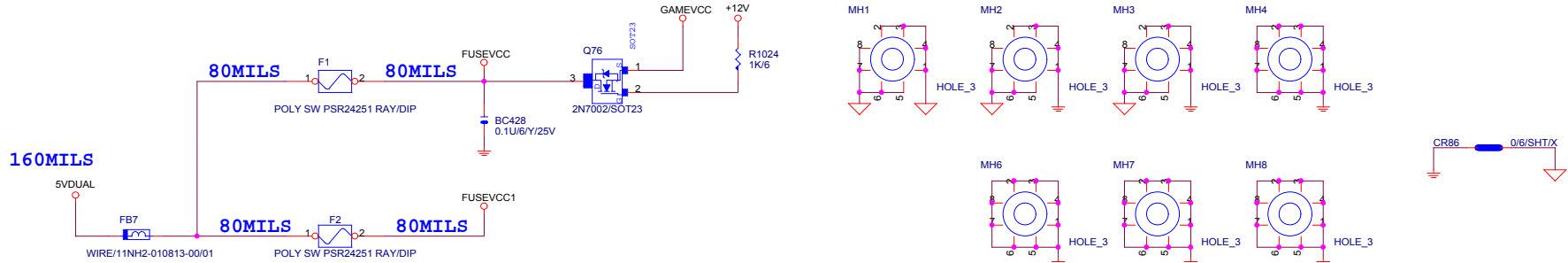
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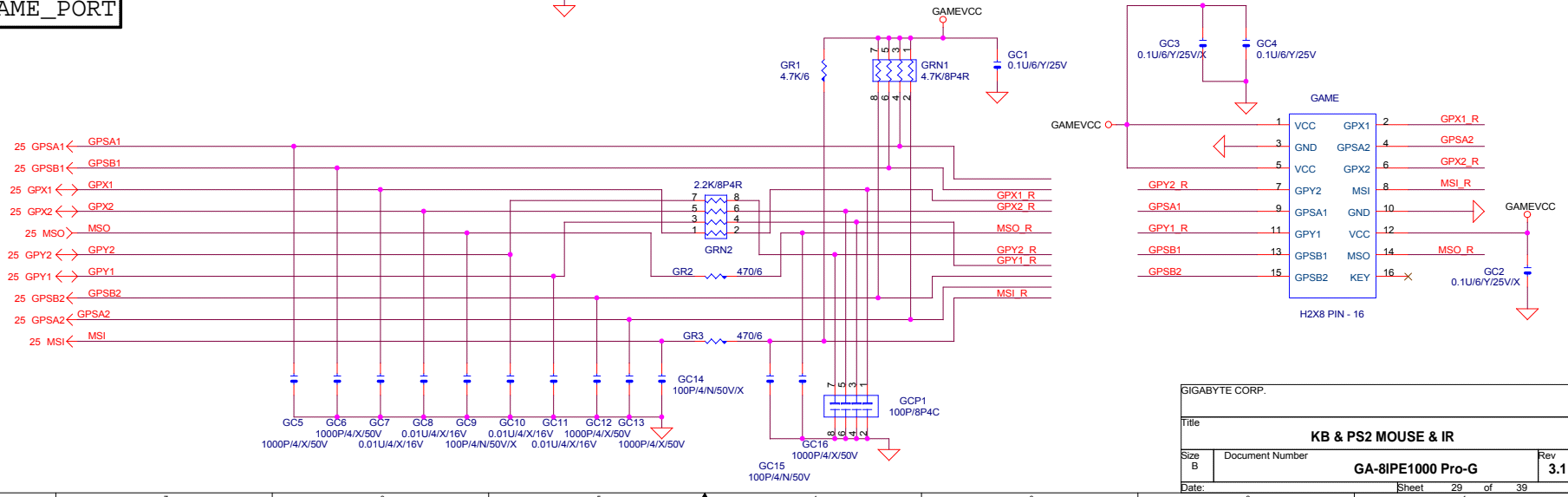
Hardware Monitor circuits



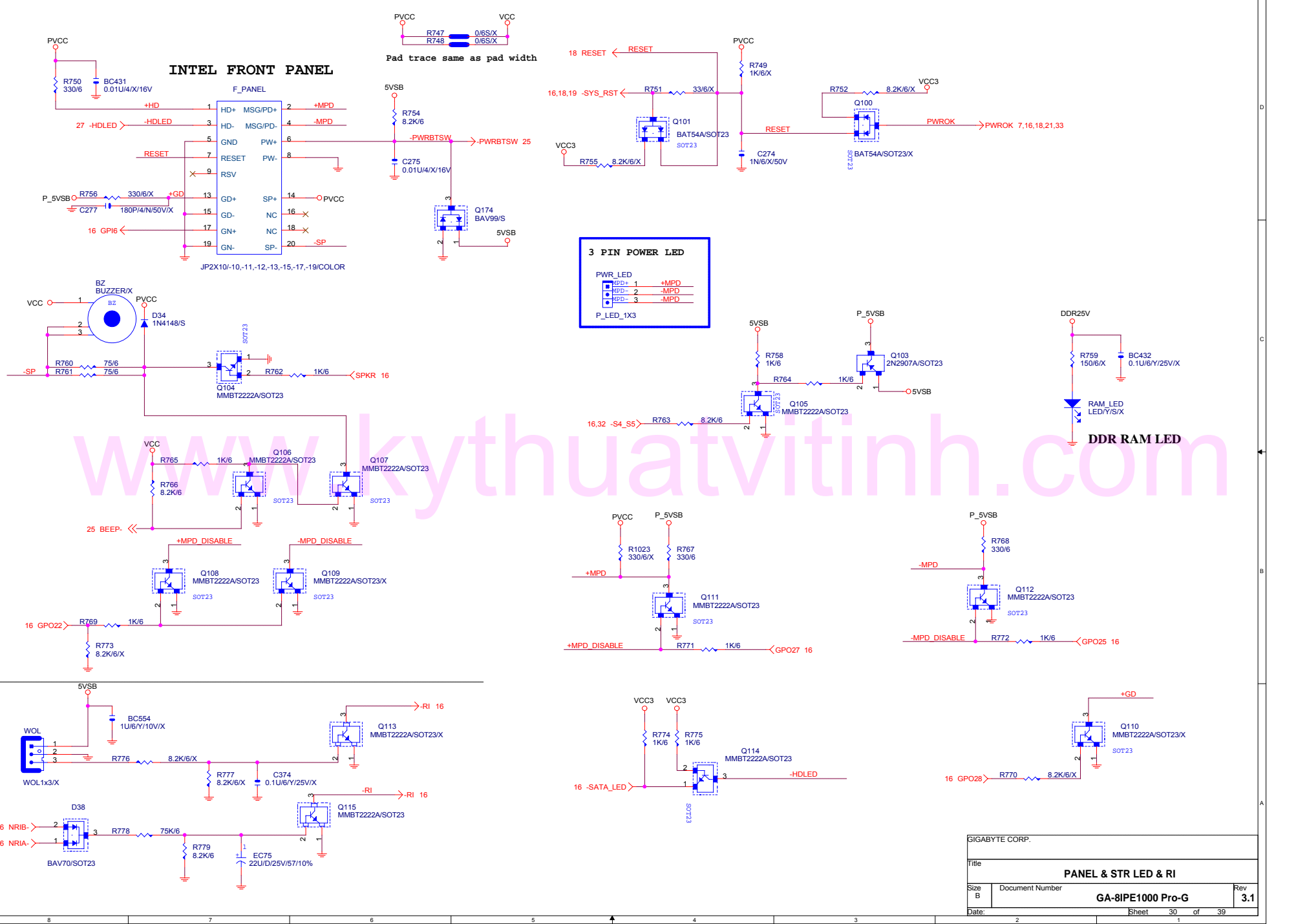
SIGABYTE CORP.		
Title		
FAN/HWMO		
Size B	Document Number	Rev
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GAME_PORT

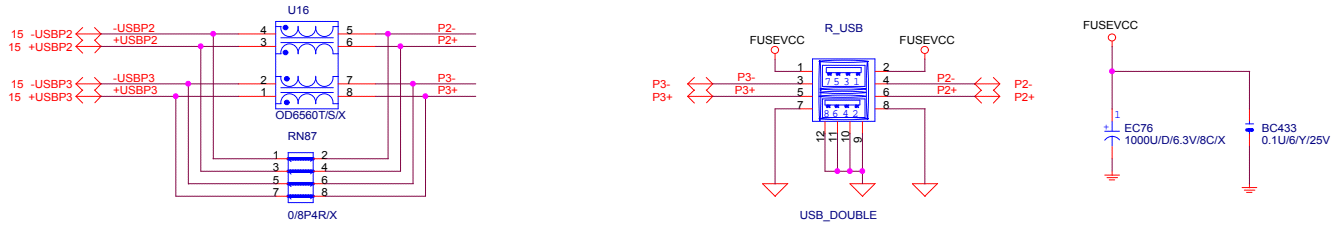


SIGABYTE CORP.		
Title		
KB & PS2 MOUSE & IR		
Size B	Document Number	Rev
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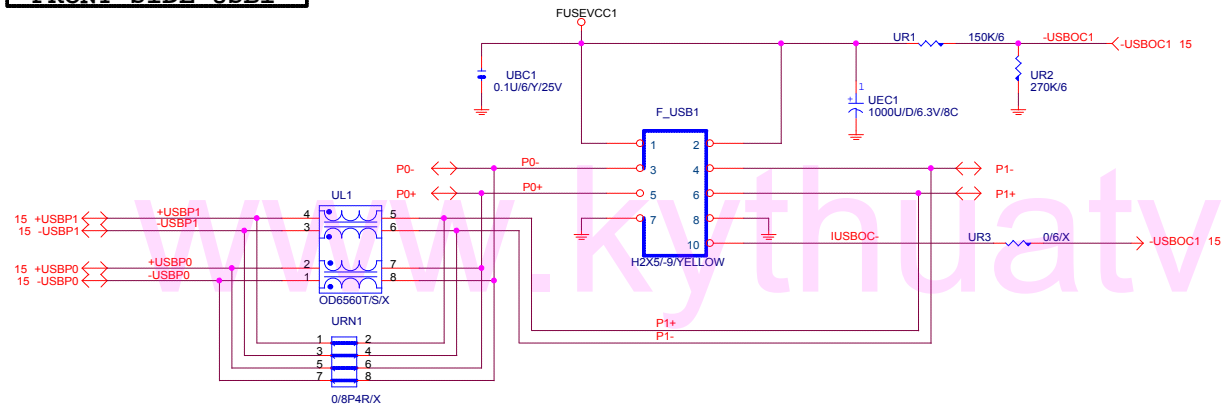


GIGABYTE CORP.		
Title		
PANEL & STR LED & RI		
Size B	Document Number	Rev
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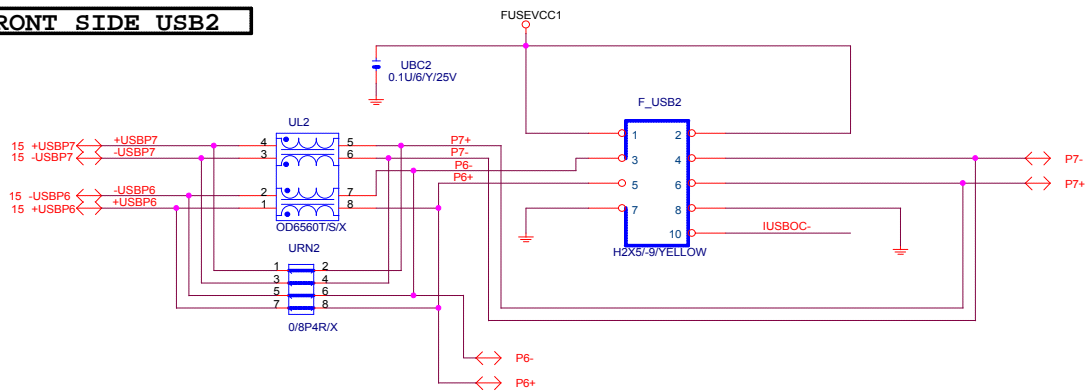
REAR USB



FRONT SIDE USB1



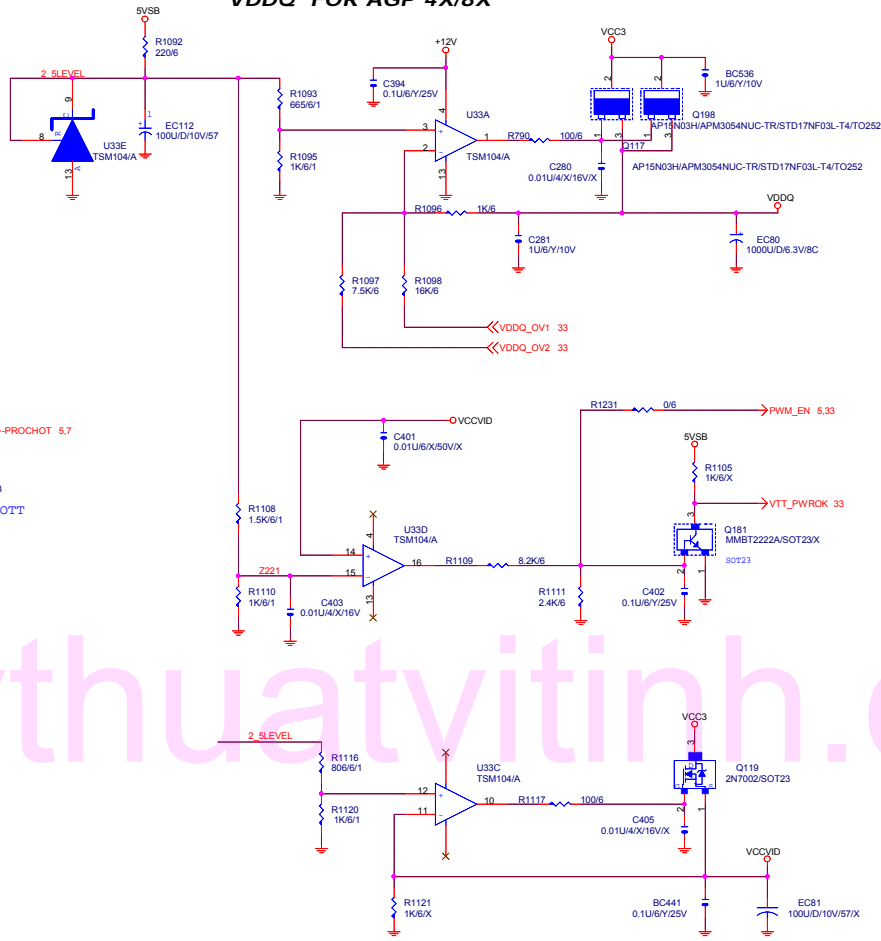
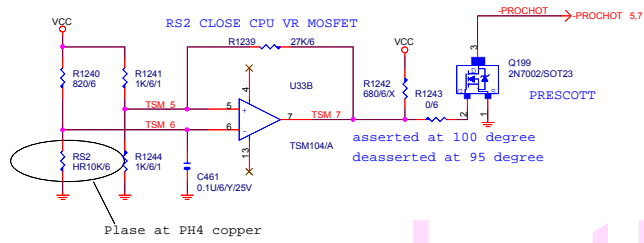
FRONT SIDE USB2



GIGABYTE CORP.		
Title		
ICH USB PORT		
Size B	Document Number	Rev
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DDR25V FOR DDR DIMM & NB

VDDQ FOR AGP 4X/8X

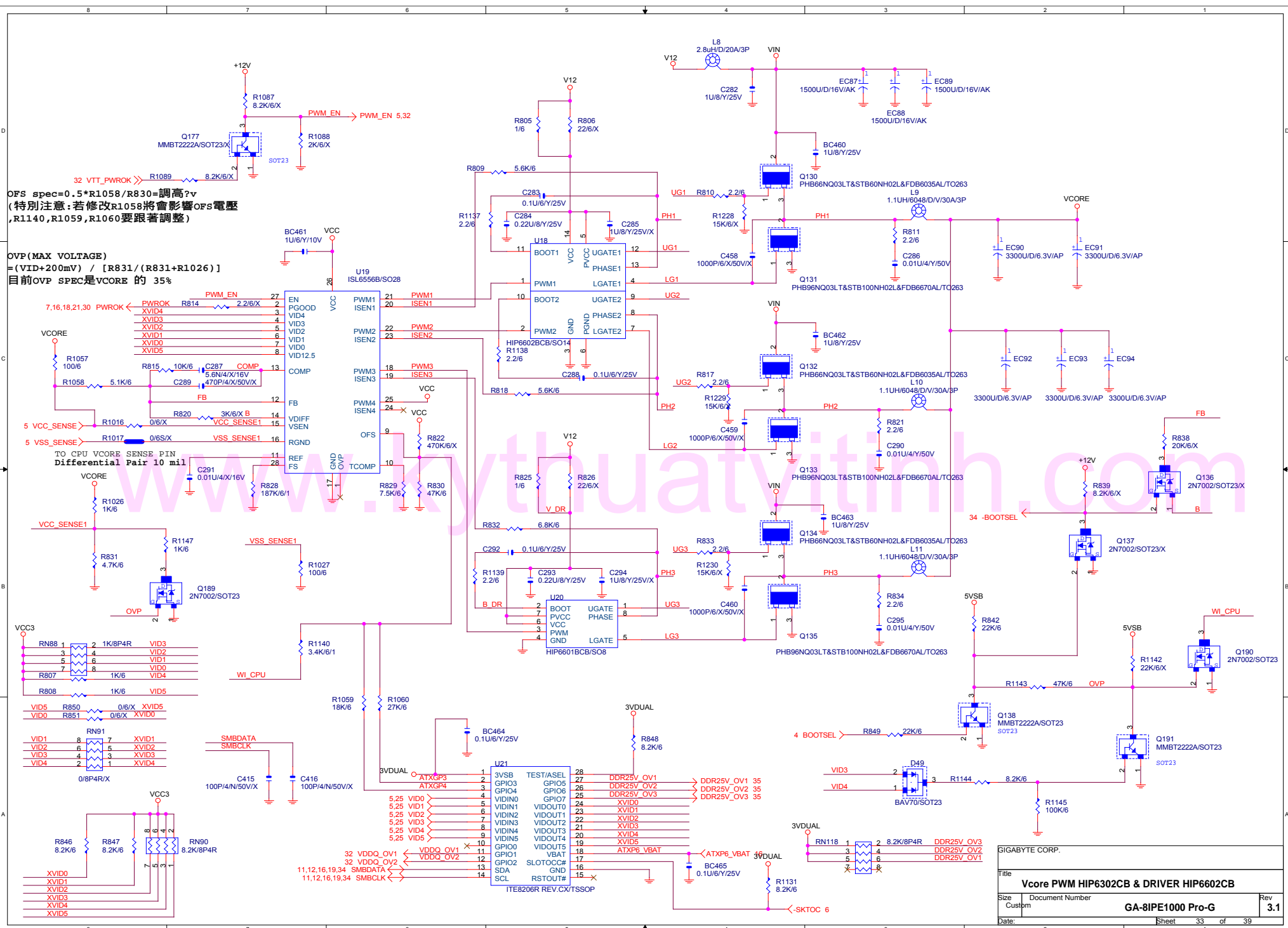


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Title		
DDR/VDDQ/VCCVID/5VDUAL POWER		
Size	Document Number	Rev
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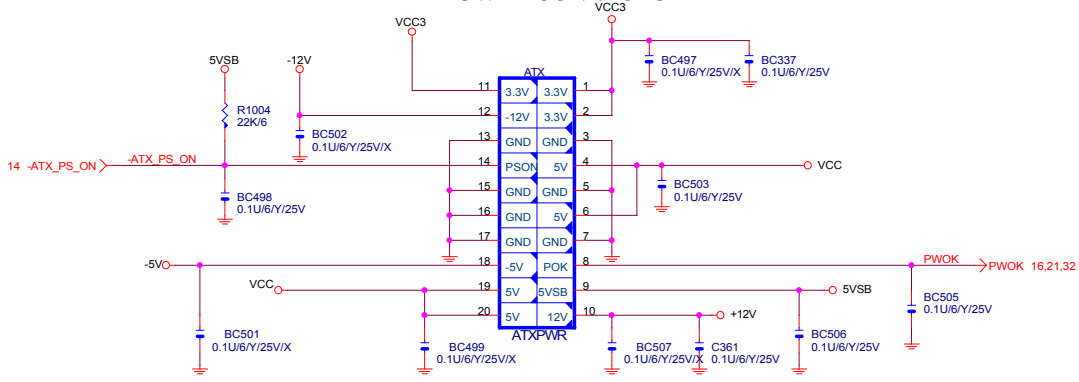
OFS spec=0.5*R1058/R830=調高?v
 (特別注意:若修改R1058將會影響OFS電壓
 ,R1140,R1059,R1060要跟著調整)

OVP(MAX VOLTAGE)
 =(VID+200mV) / [R831/(R831+R1026)]
 目前OVP SPEC是VCCORE 的 35%

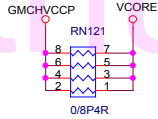
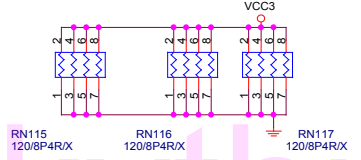
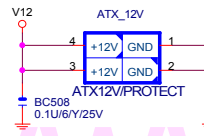
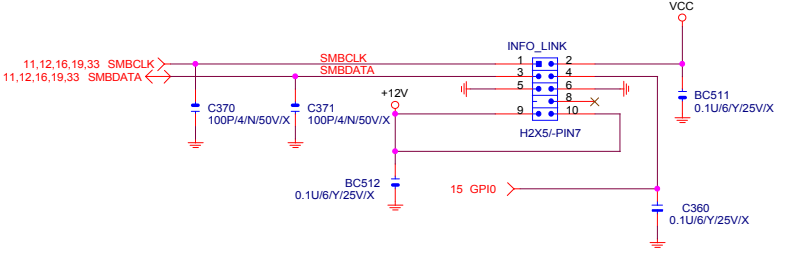


SIGNAL			
GIGABYTE CORP.			
Title Vcore PWM HIP6302CB & DRIVER HIP6602CB			
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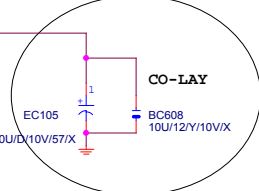
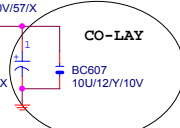
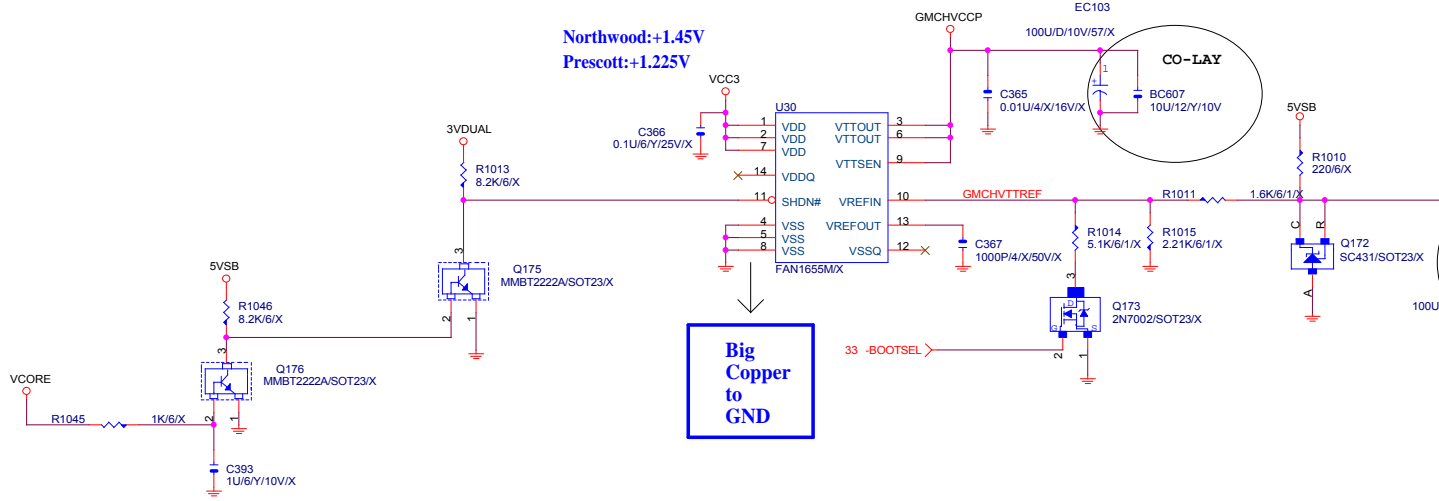
ATX POWER CONNECTOR



SMBUS CONN.

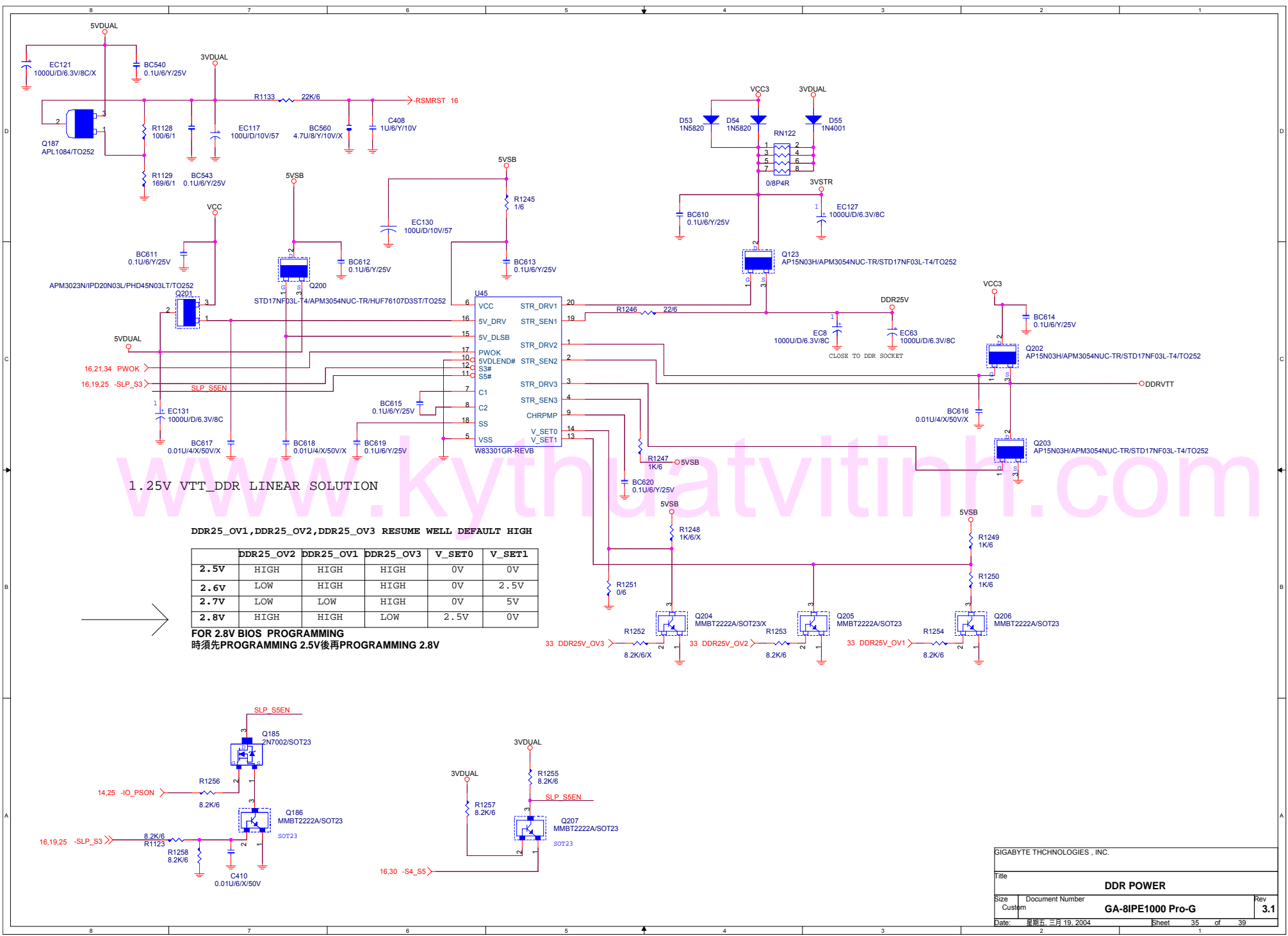


Northwood:+1.45V
Prescott:+1.225V



GIGABYTE CORP.		
Title		
Misc. PWR & ATX CONN.		
Size	Document Number	Rev
B	GA-8IPE1000 Pro-G	3.1
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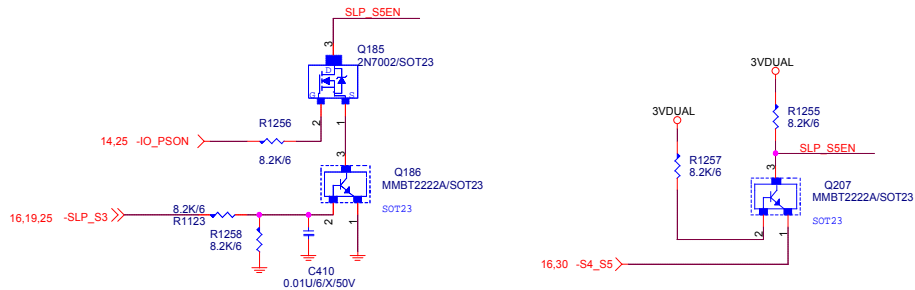
1.25V VTT_DDR LINEAR SOLUTION

DDR25_OV1,DDR25_OV2,DDR25_OV3 RESUME WELL DEFAULT HIGH

	DDR25_OV2	DDR25_OV1	DDR25_OV3	V_SET0	V_SET1
2.5V	HIGH	HIGH	HIGH	0V	0V
2.6V	LOW	HIGH	HIGH	0V	2.5V
2.7V	LOW	LOW	HIGH	0V	5V
2.8V	HIGH	HIGH	LOW	2.5V	0V

FOR 2.8V BIOS PROGRAMMING

時須先PROGRAMMING 2.5V後再PROGRAMMING 2.8V

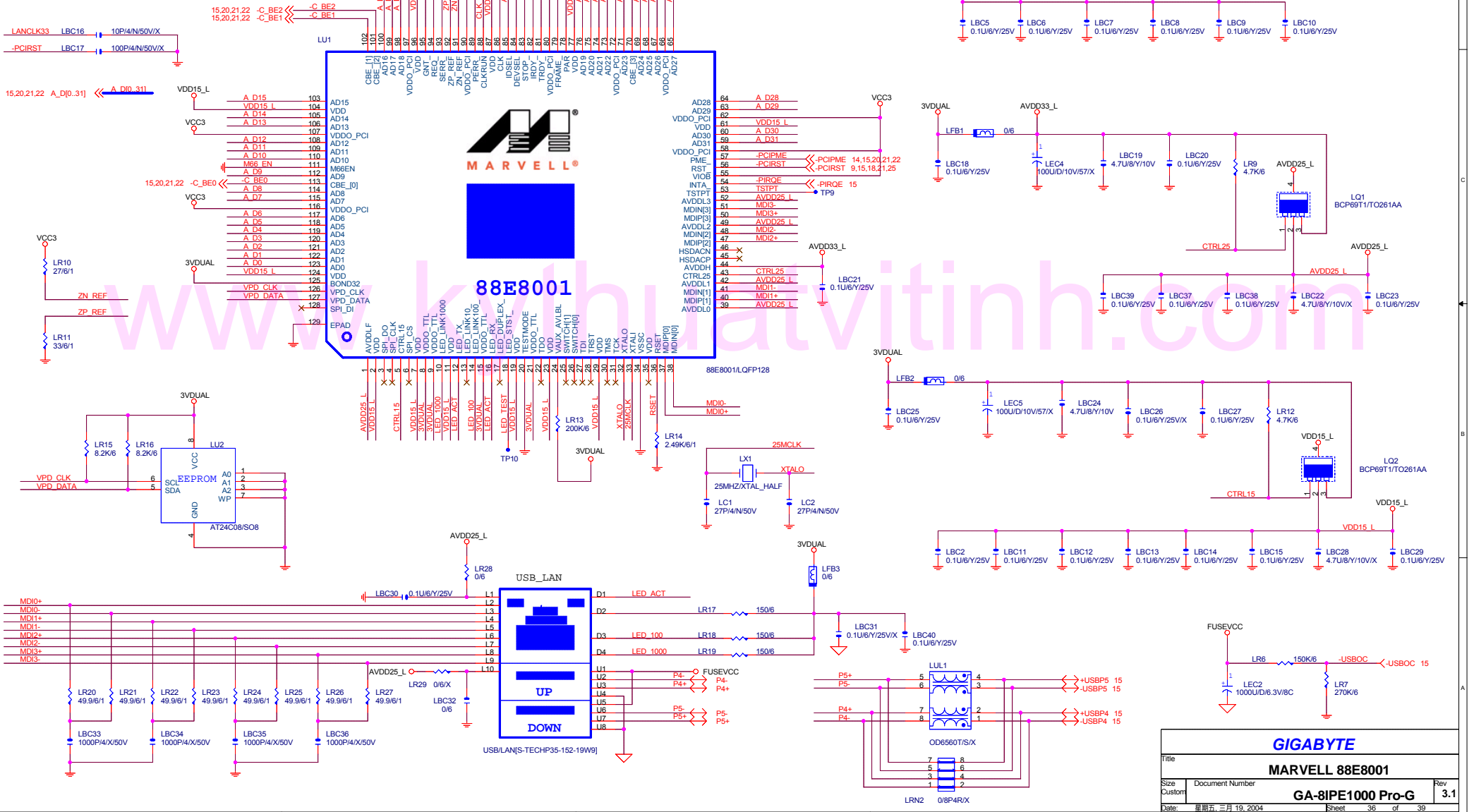


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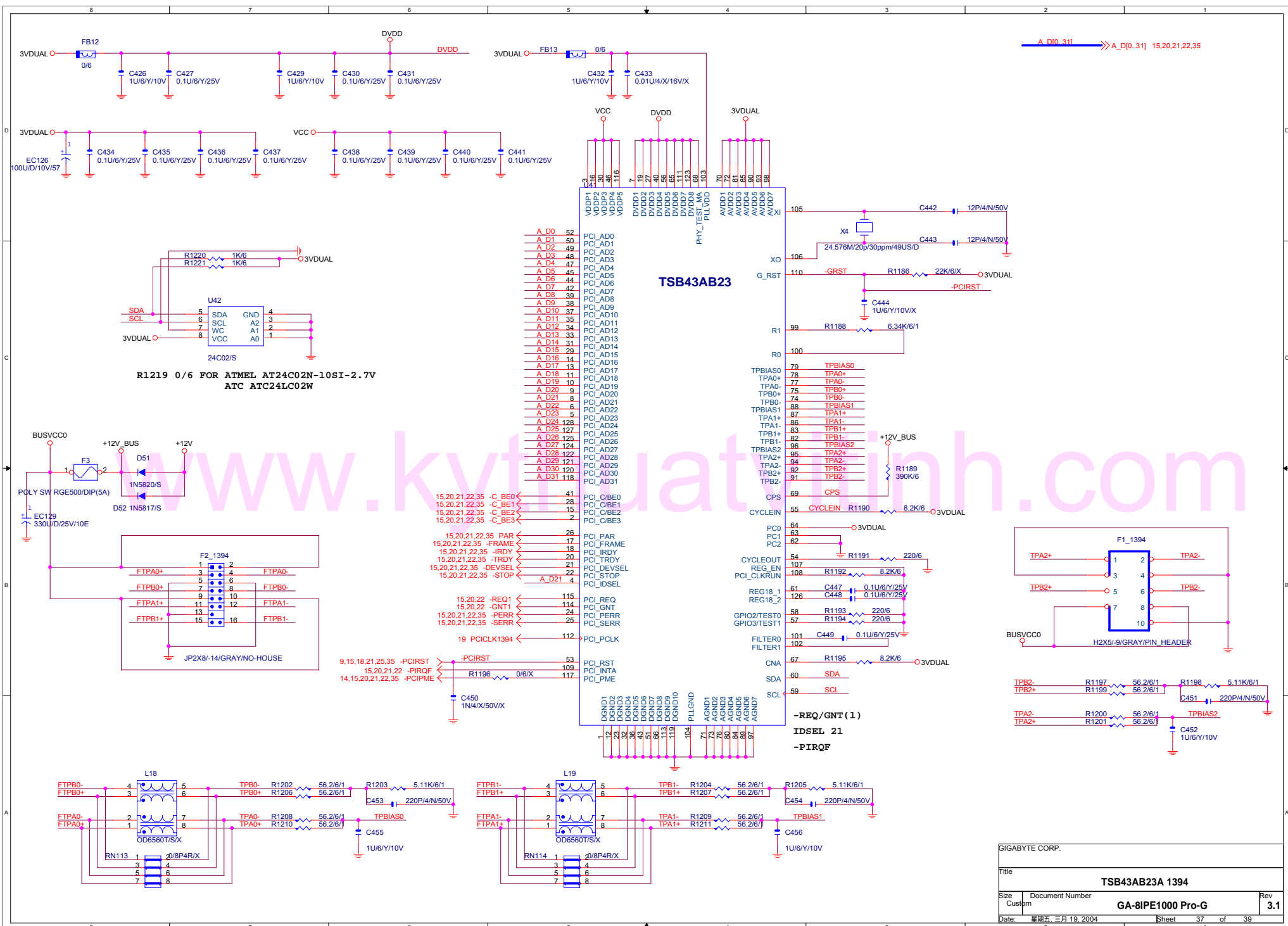
Title		DDR POWER	
Size	Document Number	GA-8IPE1000 Pro-G	
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Date:	星期五, 三月 19, 2004	Sheet	35 of 39

POWER DECOUPLING CAP.

- # Layout Check 注意事項
1. LU1 PIN129 需下內層GND, 至少打 22 VIA
 2. 3VDUAL, VCC3, VDD15_L, AVDD25_L 至少走20mil寬, 並且電容擺設每兩pin至少放一顆Bypass Cap.
 3. X'TAL 25MHz 兩訊號線, TRACE 愈短愈好, 線寬12mil
 4. MDI正負0-3, TRACE 8:7:8, 每對之間保持 40mil



GIGABYTE		
MARVELL 88E8001		
Title	Document Number	Rev
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SIBAYTE CORP.		
Title		
TSB43AB23A 1394		
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GIGABYTE GA-8IPE1000 Pro-G PCI ROUNTING LIST

PCI DEVICE	IDSEL	INT	CLOCK	REQ	GNT
PCI SLOT1	16	C,F,G,A	PCLK0	-REQ01	-GNT01
PCI SLOT2	17	F,G,A,C	PCLK1	-REQ02	-GNT02
PCI SLOT3	18	G,A,C,F	PCLK2	-REQ2	-GNT2
PCI SLOT4	19	A,C,F,G	PCLK3	-REQ3	-GNT3
PCI SLOT5	20	C,F,G,A	PCLK4	-REQ4	-GNT4
TI 1394	21	F	PCICLK1394	-REQ1	-GNT1
LAN (Marvell)	25	E	LANCLK33	-REQ5 (REQB#)	-GNT5 (GNTB#)

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Title PCI ROUNT LIST			
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Custom			
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